aiwa SERVICE

XD-DV290 K(B),EZ(B)

SERVICE MANUAL

DVD PLAYER

BASIC DVD MECHANISM : LDM-H109
(6721R-0300A)

This Service Manual is the “Revision Publishing” and replaces “Simple Manual”
K<B>:(S/M Code No.09-99C-337-5T2)
EZ<B>:(S/M Code No.09-99C-337-5T3).

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S/M Code No. 09-99C-337-5R2

REVISION DATA

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SPECIFICATIONS

DVD VIDEO PLAYER

Power supply	100V~240V, 50Hz
Power consumption	20 W
Mass	3.5kg(7.7lbs)
External dimensions	430 X 91 X 293 (W X H X D)
Signal system	NTSC
Laser	SSemiconductor laser, wavelength 655nm (DVD) /795nm (CD)
Frequency range (digital audio)	2Hz to 44kHz
Signal-to-noise ratio (digital audio)	More than 105dB (EIAJ)
Audio dynamic range (digital audio)	More than 95dB (EIAJ)
Harmonic distortion(digital audio)	0.003%
Wow and flutter	Below measurable level (less than +0.001% (W.PEAK) (EIAJ)
Operating conditions	Temperature : 5˚C(41˚F) to 35˚C(95˚F), Operation status : Horizontal

OUTPUTS

Video outputs	1.0V (p-p), 75Ω, negative sync., RCA jack x 1
S video outputs	(Y) 1.0V (p-p), 75Ω, negative sync., Mini DIN 4-pin X 1 (C) 0.286V (p-p), 75Ω
Component video output	(Y) 1.0V (p-p), 75Ω,negative sync., RCA jack X 1 (Pb)/(Pr) 0.7V (p-p), 75Ω
Audio output (digital audio)	0.5V(p-p), 75Ω, RCA jack X 1
Audio output (optical audio)	Optical connector X 1
Audio output (analog audio)	2.0Vrms (1kHz, 0dB), 330Ω, RCA jack (L, R) X 2

- Design and specifications are subject to change without notice.
- Weight and dimensions shown are approximate.

ACCESSORIES/PACKAGE LIST

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

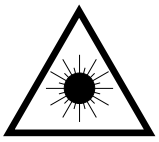
REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	S8-35R-S00-09G		INSTRUCTION ASSY
2	S8-615-20G-000		DVD-2520N CABLE ASSY
3	S7-11R-2N0-13A		REMOTE CONTROLLER A
4	S5-640-17B-000		PLUG ASSY PHONE CORD 1WAY
5	S5-640-18B-000		PLUG ASSY PHONO CORD

PROTECTION OF EYES FROM LASER BEAM DURING SERVICING

This set employs laser. Therefore, be sure to follow carefully the instructions below when servicing.

WARNING!

WHEN SERVICING, DO NOT APPROACH THE LASER EXIT WITH THE EYE TOO CLOSELY. IN CASE IT IS NECESSARY TO CONFIRM LASER BEAM EMISSION. BE SURE TO OBSERVE FROM A DISTANCE OF MORE THAN 30cm FROM THE SURFACE OF THE OBJECTIVE LENS ON THE OPTICAL PICK-UP BLOCK.



- Caution: Invisible laser radiation when open and interlocks defeated avoid exposure to beam.
- Advarsel: Usynling laserstråling ved åbning, når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

VAROITUS!

Laiteen Käyttäminen muulla kuin tässä käyttöohjeessa mainitulla tavalla saattaa altistaa käyt-täjän turvallisuusluokan 1 ylittävälle näkymättömälle lasersäteilylle.

VARNING!

Om apparaten används på annat sätt än vad som specificeras i denna bruksanvising, kan användaren utsättas för osynling laserstrålning, som överskrider gränsen för laserklass 1.

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

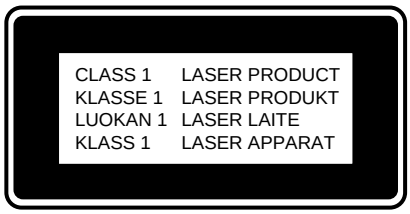
ATTENTION

L'utilisation de commandes, réglages ou procédures autres que ceux spécifiés peut entraîner une dangereuse exposition aux radiations.

ADVARSEL!

Usynlig laserstråling ved åbning, når sikkerhedsafbrydereer ude af funktion. Undgå udsættelse for stråling.

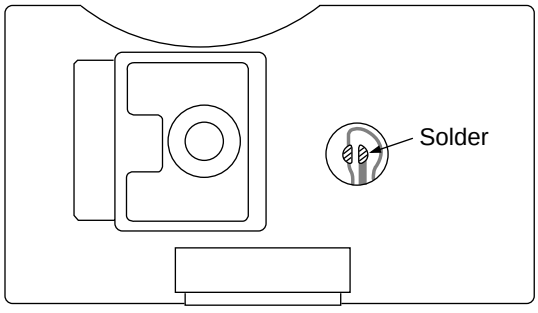
This Compact Disc player is classified as a CLASS 1 LASER product.
The CLASS 1 LASER PRODUCT label is located on the rear exterior.



Precaution to replace Optical block (LPC-512A)

Body or clothes electrostatic potential could ruin laser diode in the optical block. Be sure ground body and workbench, and use care the clothes do not touch the diode.

1) After the connection, remove solder shown in the right figure.



DISASSEMBLY INSTRUCTIONS

CAUTION BEFORE STARTING SERVICING

Electronic parts are susceptible to static electricity and may easily damaged, so do not forget to take a proper grounding treatment as required.
Many screws are used inside the unit. To prevent missing, dropping, etc. of the screws, always use a magnetized screw driver in servicing. Several kinds of screws are used and some of them need special cautions. That is, take care of the tapping screws securing molded parts and fine pitch screws used to secure metal parts. If they are used improperly, the screw holes will be easily damaged and the parts can not be fixed.

CABINET DISASSEMBLY

1. Top Case

1) Release 7 screws (A). (See Fig-1)
2) Lift the top case with holding the back of it, and remove it in the direction of the arrow.

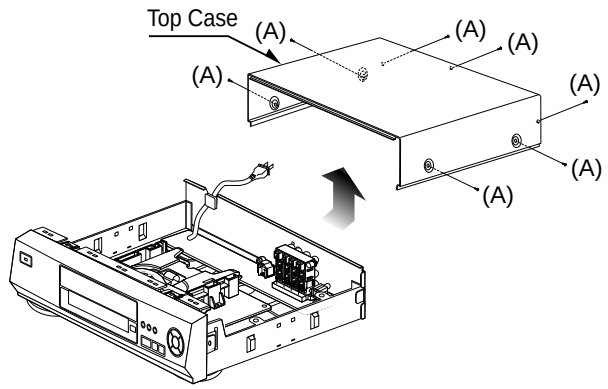


Fig-1

2. Tray Door

1) Eject the disc tray.
2) Lift up the tray door in the direction of the arrow.

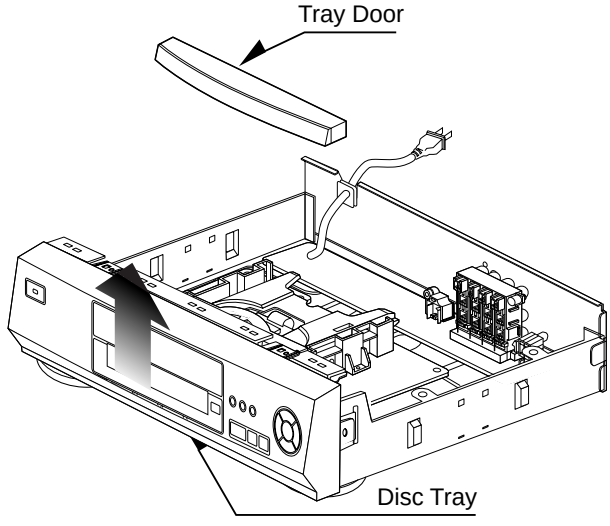


Fig-2

3. Front Panel

1) Eject the disc tray. (See Fig-2)
2) Remove the tray door. (See Fig-2)
3) Release 2 screws (B).
4) Pull the front panel toward you while pressing 7 stoppers to disengage, and remove the front panel. (See Fig-3)

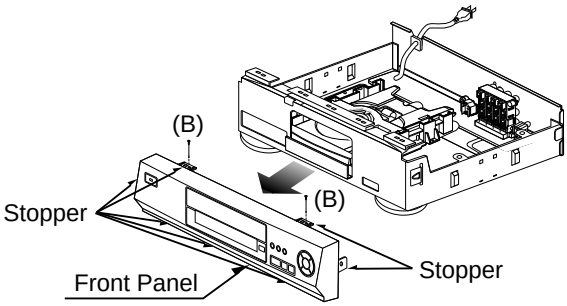


Fig-3

CIRCUIT BOARD DISASSEMBLY

Note: Before removing the main circuit board, be sure to shortcircuit the laserdiode output land.
After replacing the main circuit board, open the land after inserting the flexible connector.
(Refer to Mechanism Disassembly)

4. Main/JACK C.B

1) Remove the top case. (See Fig-1)
2) Release 10 screws (C), and take out the main/JACK C.B. (See Fig-4)
3) Remove the flexible connectors and the connector from main circuit board.
4) Then, remove the main JACK C.B.

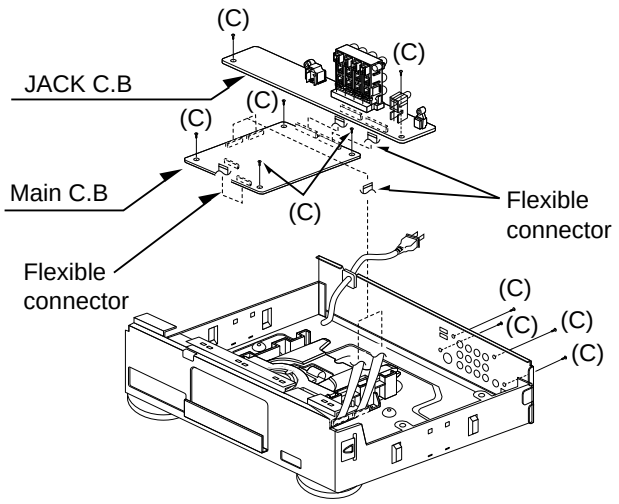


Fig-4

5. Power C.B

1) Release 4 screws (D). (See Fig-5)

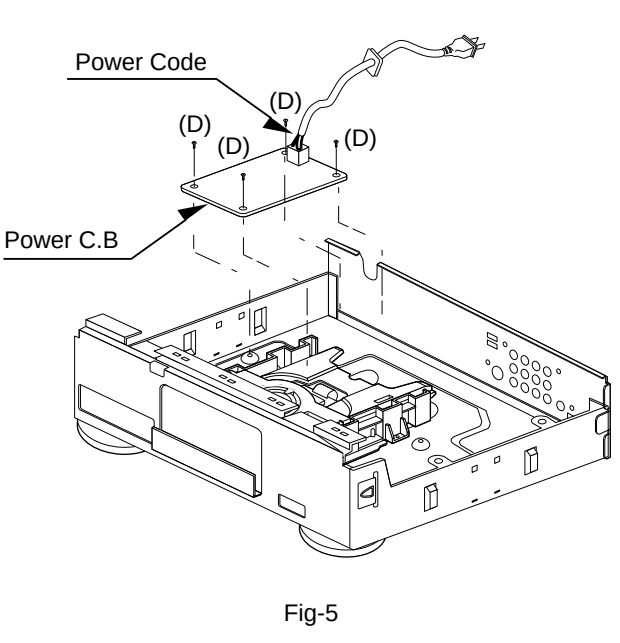


Fig-5

6. TIMER and Key C.B

1) Remove the front panel. (See Fig-3)
2) Release 5 screws (E), and remove the TIMER C.B.

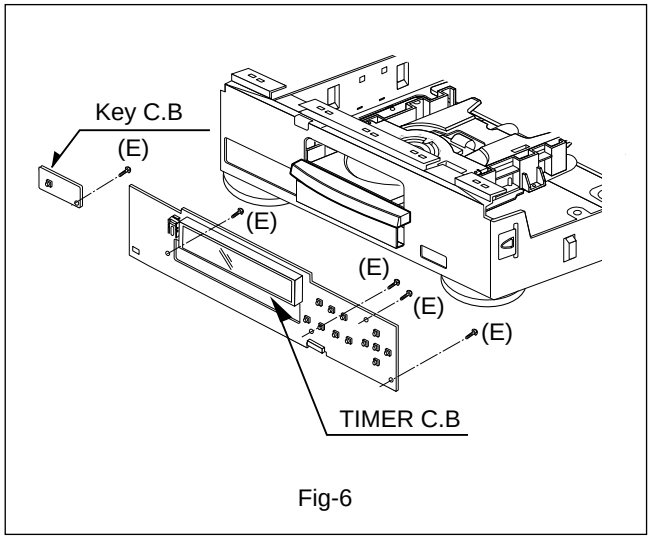
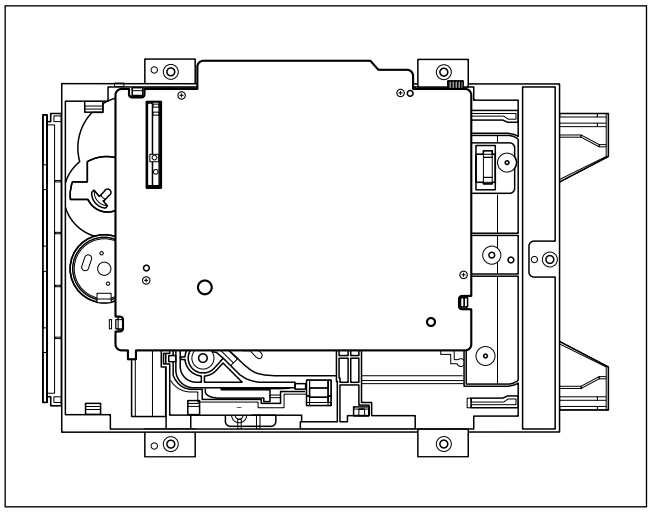


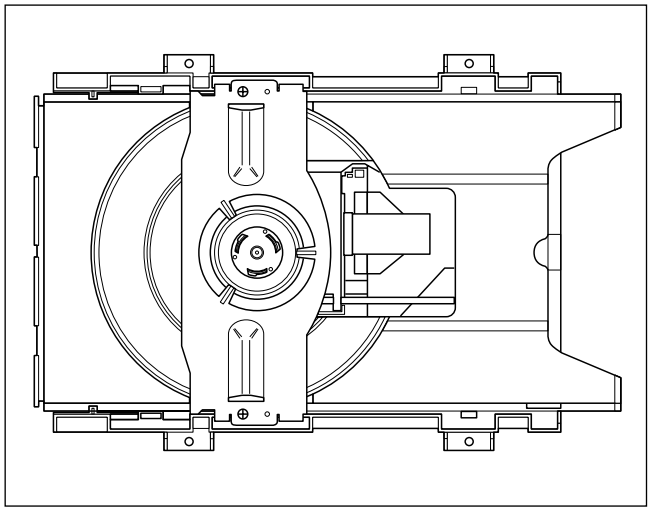
Fig-6

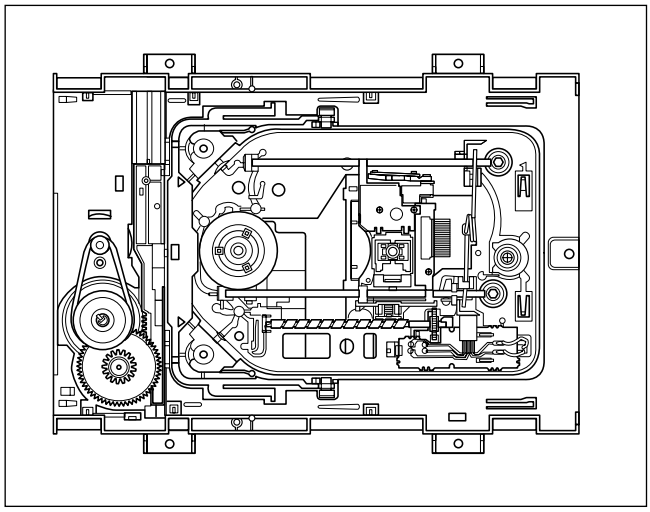
DECK MECHANISM PARTS LOCATION

• Bottom View



• Top View





Procedure Starting No.		Parts	Fixing Type	Disassembly	Figure
	1	Junction P.C.Board	4 Screws, 4 Locking Tabs	Bottom	4-1
	2	Bracket Assembly Clamp	2 Screws		4-2
	3	Bracket Clamp			4-2
	4	Clamp Assembly Disk			4-2
	5	Plate Clamp			4-2
5	6	Magnet Clamp			4-2
5, 6	7	Clamp Lower			4-2
2	8	Tray Disk	1 Locking Tab		4-3
2, 8	9	Base Assembly Feed	1 Connector		4-4
2, 8	10	Rubber R	1 Screw		4-4
2, 8	11	Spring Skew	1 Hook		4-4
2, 8, 11	12	Shaft PU Main			4-4
2, 8, 11	13	Shaft PU Sub			4-4
2, 8, 12, 13	14	Mechanism Assembly PU Unit			4-4
2, 8, 12-14	15	Guide Freed PU	1Screw		4-4
2, 8, 12-14	16	Spring Guide Feed			4-4
2, 8, 12-16	17	Pick up Assembly General			4-4
2, 8, 9	18	Motor (Mech.)	3Screws	Bottom	4-4
2, 8, 9	19	Shaft Lead Screw			4-4
2, 8, 9	20	Motor Assembly PU Freed	2 Locking Tabs	Bottom	4-4
2, 8, 9-20	21	Base PU (Outsert)			4-4
1, 2, 8, 9	22	Base Assembly Main			4-5
1, 2, 8, 9	23	Holder Assembly Deck on	1 Locking Tab	Bottom	4-5
2, 8, 9	24	Frame Assembly Up/Down	2 Locking Tabs		4-5
2, 8, 9	25	Rubber F			4-5
2, 8	26	Belt Loading			4-5
2, 8, 26	27	GearPulley	1 Screw		4-5
2, 8, 26, 27	28	Gear Loading			4-5
2, 8, 26-28	29	Gear Emergency			4-5
2, 8, 26-29	30	Cam Loading			4-5
1, 2, 8, 26-30	31	Motor Assembly Loading	2 Screws	Bottom	4-5
1, 2, 8, 26-31	32	Base Main	1 Locking Tab		4-5

Note: When reassembling, perform the procedure in reverse order. The “Bottom” on Disassembly column of above Table indicates the part should be disassembled at the Bottom side.

DECK MECHANISM ASSEMBLY

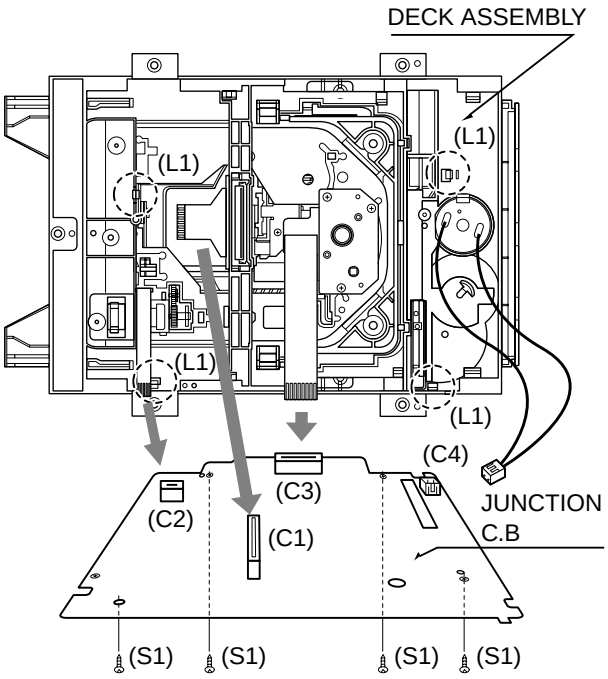


Fig-7

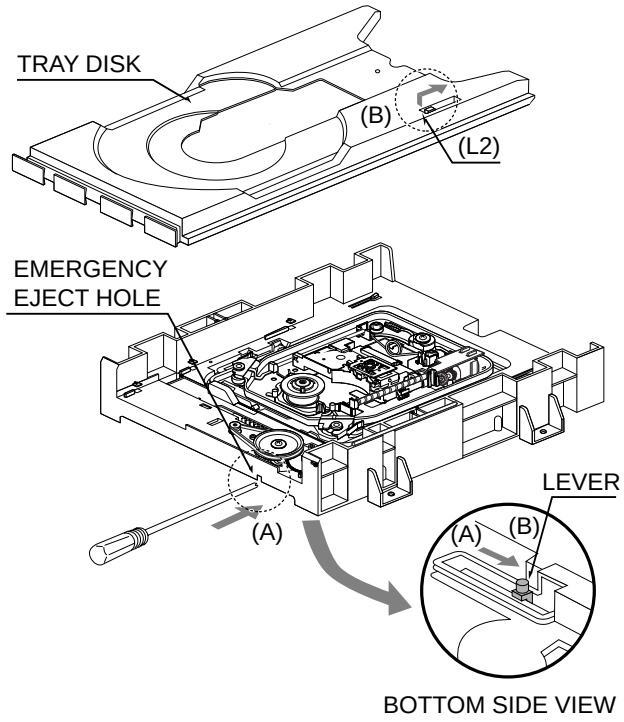


Fig-9

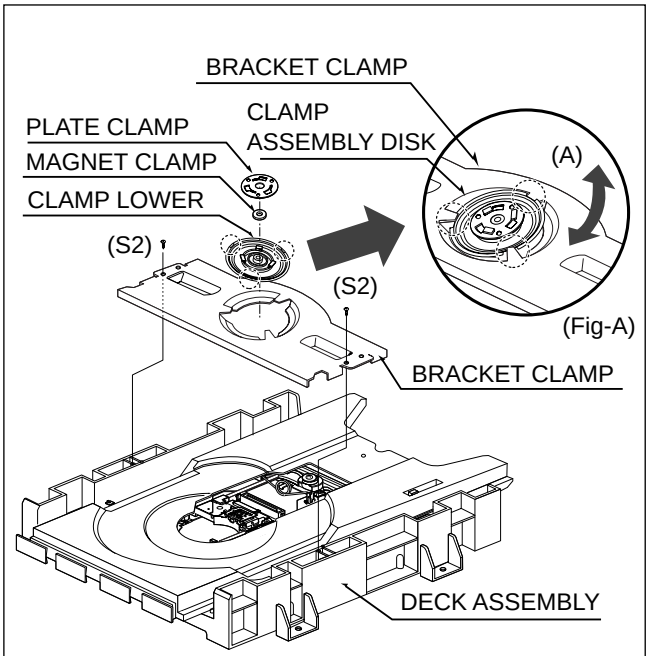


Fig-8

7. Junction C.B (Fig-7)

1) Put the Deck Assembly face down. (Bottom side)
2) Release 4 Screws (S1).
3) Unlock 4 Locking tabs (L1).
4) Lift up the Junction C.B a little to disconnect the Connector (C1).
5) Disconnect 3 Connectors (C2, C3, C4).

8. Bracket Assembly Clamp (Fig-8)

1) Put the Deck Assembly on original position. (Top side)
2) Release 2 Screws (S2).
3) Lift up the Bracket Assembly Clamp.

8-1. Clamp Assembly Disk

1) Place the Clamp Assembly Disk as Fig-(A).
2) Lift up the Clamp Assembly Disk in direction of arrow (A).
3) Separate the Clamp Assembly Disk from the Bracket Clamp.

8-1-1. Plate Clamp

1) Turn the Plate Clamp to counterclockwise direction and then lift up the Plate Clamp.

8-1-2. Magnet Clamp

8-1-3. Clamp Lower

8-2. Bracket Clamp

9. Tray Disk (Fig-9)

1) Insert and push a Driver in the emergency eject hole (A) at the front side, or put the Driver on the Lever (B) of the Gear Emergency and pull the Lever (B) in direction of arrow (A) so that the Tray Disk is ejected about 15-20mm.
2) Pull the Tray Disk until the moving is locked by the Locking Tab (L2).
3) Unlock the Locking tab (L2) in direction of arrow (B).
4) Separate the Tray Disk completely.

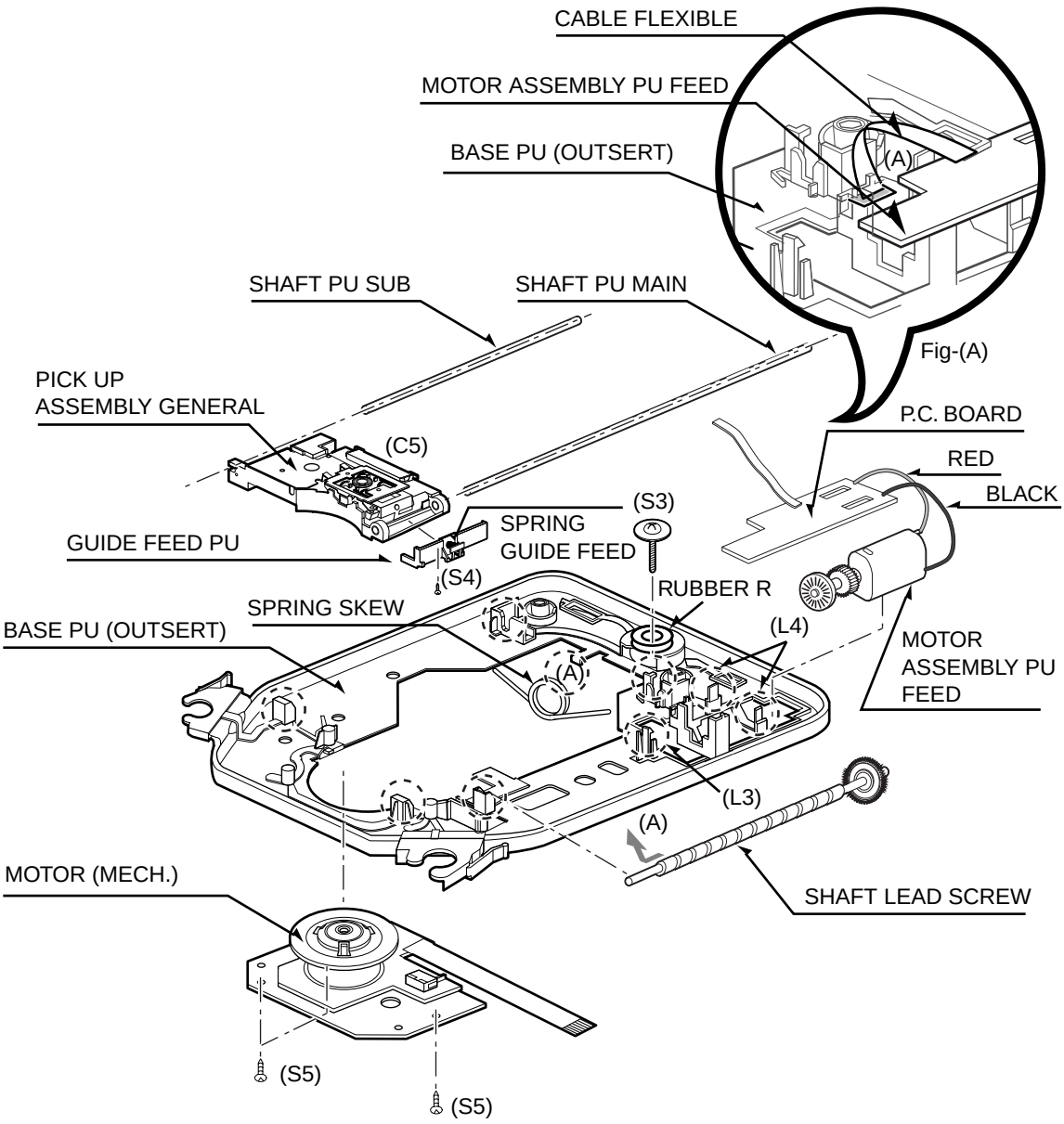


Fig-10

10. Base Assembly Feed (Fig-10)

1) Disconnect the Connector (C5)
2) Release the Screw (S3).

10-1. Rubber R

10-2. Spring Skew

1) Press the (A) position of the Spring Skew and unlock the Spring Skew locking.

10-3. Shaft PU Main

10-4. Shaft PU SUB

Note: When reassembling, be careful not to change the Shaft PU Main (Long) and the Shaft PU Sub (Short).

10-5. Mechanism Assembly PU Unit

10-5-1. Guide Feed PU

1) Release the Screw (S4) and separate the Guide Feed PU from the Pick up Assembly General.

10-5-2. Spring Guide Feed

10-5-3. Pick Up Assembly General

10-6. Motor (mech.)

1) Release the 3 Screws (S5) at bottom side.
2) Push down the Motor (Mech.) and separate from the Base PU (Outsert).

10-7. Shaft Lead Screw

1) Push the Shaft Lead Screw in direction on arrow (A) a little and lift up the Shaft Lead Screw.

10-8. Motor Assembly PU Feed.

1) Unlock the Locking tab (L3) and lift up the P.C.Board.
2) Unlock two Locking Tabs (L4) and push down the Motor Assembly PU Feed.
3) Separate the Motor Assembly PU Feed from the Base PU (Outsert).

Note: When reassembling, place the Motor Assembly PU Feed as Fig-(A) and insert the Cable Flexible to the Hole (A) of the Base PU (Outsert). (See Fig-(A))

10-9. Motor (mech.)

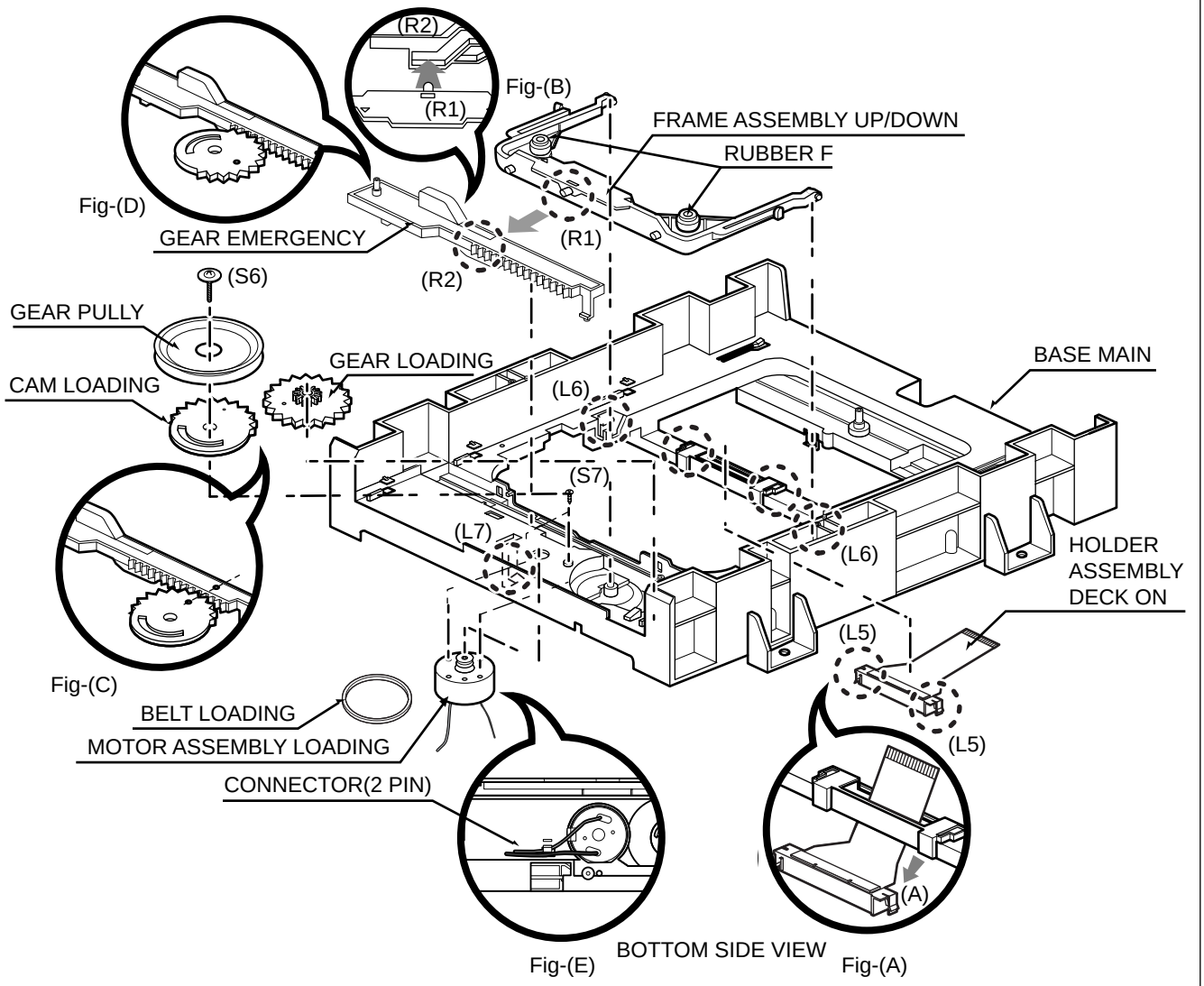


Fig-11

11. Base Assembly Main (Fig-11)

11-1. Holder Assembly Deck On

1) Push the Locking tabs (L5) at bottom side of the Holder Assembly Deck On in direction of arrow (A) and separate to bottom side. (See Fig-(A))

11-2. Frame Assembly Up/Down.

1) Push the two Locking tabs (L6) and lift up the Frame Assembly Up/Down.

Note: When reassembling, insert the Lever (R1) of the Frame Assembly Up/Down to the Groove (R2) of the Gear Emergency and lock the two Locking Tabs (L6). (See Fig-(B))

11-3. Rubber F

11-4. Belt Loading

11-5. Gear Pulley

1) Release the Screw (S6) and lift up the Gear Pulley.

11-6. Gear Loading

11-7. Gear Emergency

Note: When reassembling, confirm that the Hole (A) of the Cam Loading is aligned to the Hole (B) of the Gear Emergency as Fig-(C).
For this alignment, place the Gear Emergency and Cam Loading as Fig-(D), and then move the Gear Emergency in direction of arrow (B) until these two gears are aligned as Fig-(C).

11-8. Cam Loading

11-9. Motor Assembly Loading

1) Release two Screws (S7).
2) Unlock the Locking tab (L7) and separate the Motor Assembly Loading to bottom side.

Note: When reassembling, confirm that the Connector (2 Pin) is aligned as Fig-(E)

11-10. Base Main

ELECTRICAL MAIN PARTS LIST

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
IC			
	SI-AM2-980-01A		IC,AM29F800B-120EC
	SI-AL2-402-10E		IC,AT24C02N-10SC-2.7
	SI-AL4-981-92B		IC,AT49F8192A-90TC
	SI-RH5-983-20A		IC,BA5983FP-E2
	SI-RH6-859-20A		IC,BA6859AFP-E2
	SI-RW8-610-00A		IC,BT861
	SI-HY2-580-10A		IC,GDC25D801AA
	SI-GS7-142-60E		IC,GM71C4260CJ-60
	SI-HI6-417-03B		IC,HD6417034AFI20
	SI-SS4-310-00A		IC,KA431AZ
	SI-SS7-542-00A		IC,KA7542Z
	SI-SS7-808-00H		IC,KA78R08 4P
	SI-KE3-930-00G		IC,KIA393F-EL
	SI-KE4-310-00A		IC,KIA431 3P
	87-001-196-010		IC,KIA7042P
	SI-SS4-161-02F		IC,KM4161020CT-G7
	SI-SA8-661-12C		IC,LC866112B-5N21
	SI-JR3-414-00C		IC,NJM3414AM-TE1,3K/REEL
	SI-JR4-580-00B		IC,NJM4580M
	SI-BB1-716-00A		IC,PCM1716E 28P
	SI-BB1-700-00A		IC,PLL1700E 20P
	SI-SH2-050-00A		IC,PQ20WZ5U 20WZ51
	SI-SH3-130-00A		IC,PQ3DZ13U
	SI-TI7-437-40K		IC,SN74AHC374PWLE
	SI-SK6-153-00A		IC,STR-G6153T 5P
	SI-TO1-254-00B		IC,TA1254AF
	SI-TO1-254-00A		IC,TA1254F
	SI-TO7-040-00F		IC,TC7W04FU
	SI-MQ5-316-25A		IC,V53C16256HK50
	SI-CU3-000-00A		IC,ZIVA3-PE0
	SI-GS7-216-16C		ICGM72V161621ET-7
TRANSISTOR			
	ST-R10-500-9AD		TR,KRA105M
	ST-R10-300-9AE		TR,KRC103M
	ST-R10-500-9AB		TR,KRC105M
	ST-R11-510-0AA		TR,KSB1151-Y
	ST-R12-670-9AC		TR,KTA1267-GR
	ST-R15-040-9BF		TR,KTA1504S-Y
	ST-R15-050-9AD		TR,KTA1505S-Y
	ST-R31-980-9AC		TR,KTC3198-TP-BL
	ST-R13-040-9BA		TR,KTD1304S
	ST-R10-000-9CB		TR,UMX1N
	ST-R10-000-9BM		TR,UMZ1N 3K
	87-070-334-070		ZENER,MTZ10B
	SM-TZ6-8CT-000		ZENER,MTZ6.8C
DIODE			
	SD-D19-300-9AB		C-DIODE,KDS193
	ST-R10-370-9BB		C-TR,2SA1037K-Q
	ST-R10-300-9AA		C-TR,KRC103S-T1
	ST-R38-750-9AC		C-TR,KTC3875S-GR-T1
	SD-R15-402-0BA		DIODE,1N5402
	87-020-465-080		DIODE,1SS133
	SD-R10-451-0AA		DIODE,B10A45V1
	SD-D01-000-9CA		DIODE,EG01CW
	SD-R18-020-9AA		DIODE,ERA18-02KFRB
	87-A40-284-080		DIODE,ERA22-10
	SD-D01-000-9AC		DIODE,EU01W
	83-NEG-677-080		DIODE,MTZ5.6B
	SD-R49-500-9AA		DIODE,RB495D
	87-017-352-010		DIODE,RU3YXLF-C1 100V2
	87-070-173-010		DIODE,S1WBA60
MAIN C.B			
	C204	SC-H71-06C-611	C-CAP,10UF-6.3V
	C207	SC-H71-06C-611	C-CAP,10UF-6.3V
	C213	SC-H71-06C-611	C-CAP,10UF-6.3V
	C214	SC-H71-06C-611	C-CAP,10UF-6.3V
	C215	SC-H71-06C-611	C-CAP,10UF-6.3V
	C216	SC-H71-06C-611	C-CAP,10UF-6.3V
	C218	SC-H71-06C-611	C-CAP,10UF-6.3V
	C219	SC-H71-06C-611	C-CAP,10UF-6.3V
	C220	SC-H81-07C-621	C-CAP,100UF-6.3V
	C224	SC-H71-06C-611	C-CAP,10UF-6.3V
	C226	SC-H71-06C-611	C-CAP,10UF-6.3V
	C230	SC-H71-06C-611	C-CAP,10UF-6.3V
	C302	SC-H81-07C-691	C-CAP,100UF-6.3V
	C310	SC-H71-06F-621	C-CAP,10UF-16V
	C311	SC-H71-06F-621	C-CAP,10UF-16V
	C708	SC-H71-06C-611	C-CAP,10UF-6.3V
	C709	SC-H82-27D-611	C-CAP,220UF-10V
	C712	SC-H71-06C-611	C-CAP,10UF-6.3V
	C713	SC-H71-06C-611	C-CAP,10UF-6.3V
	C714	SC-H71-06F-621	C-CAP,10UF-16V
	C718	SC-H71-06C-611	C-CAP,10UF-6.3V
	CE201	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE202	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE203	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE205	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE206	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE210	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE211	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE221	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE223	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE228	SC-H84-76C-611	C-CAP,47UF-6.3V
	CE609	SC-H81-07F-611	C-CAP,100UF-16V
	CE610	SC-H81-07F-611	C-CAP,100UF-16V
	CE710	SC-H84-76C-611	C-CAP,47UF-6.3V
	X101	S2-12H-B20-02A	CCR20.0MC6T TDK 20000000H
	X301	S2-02R-427-01G	C-RESO 27MHZ 20P
JUNCTION C.B			
	CE450	87-010-140-080	CAP,E 47-16V
	CE451	87-010-140-080	CAP,E 47-16V
	CE452	87-010-140-080	CAP,E 47-16V
	CE453	87-010-140-080	CAP,E 47-16V
	R451	SR-D01-01H-633	RES,1-1/2W
	R452	SR-D01-01H-633	RES,1-1/2W
TIMER C.B			
	C500	SC-E22-73D-638	CAP,E 220-10V
	C502	SC-E10-63F-638	CAP,E 10-16V
	C506	SC-E47-63J-638	CAP,E 47UF-35V
	C507	SC-E10-63F-638	CAP,E 10-16V
	C512	87-010-140-080	CAP,E 47-16V
	C513	87-010-140-080	CAP,E 47-16V
	DIG501	S3-02H-V00-1D0	7-BT-259GK DH
	LED501	SD-L32-531-9AA	LED SPR325MVWT31(GRN)
	RC501	S7-12R-083-8GA	TSOP1238UQ1 TEMIC 8MM 37 RC
	SW501	S5-562-19B-000	SW,SKHV10910B
	SW502	S5-562-19B-000	SW,SKHV10910B
	SW503	S5-562-19B-000	SW,SKHV10910B
	SW503	S5-562-19B-000	SW,SKHV10910B
	SW504	S5-562-19B-000	SW,SKHV10910B
	SW505	S5-562-19B-000	SW,SKHV10910B
	SW506	S5-562-19B-000	SW,SKHV10910B
	SW507	S5-562-19B-000	SW,SKHV10910B
	SW510	S5-562-19B-000	SW,SKHV10910B
	SW511	S5-562-19B-000	SW,SKHV10910B
	SW512	S5-562-19B-000	SW,SKHV10910B
	SW513	S5-562-19B-000	SW,SKHV10910B

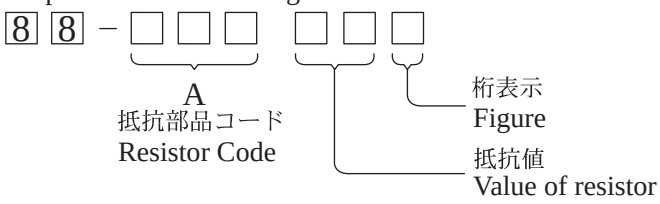
REF. NO	PART NO.	KANRI NO.	DESCRIPTION
SW514	S5-562-19B-000		SW,SKHV10910B
X501	S6-160-20P-000		CSA6.00MGU MURATA 6MHZ
JACK C.B			
CV1	87-010-060-080		CAP,E 100-16V
CV2	SC-E22-76F-638		CAP,E 220UF-16V
CV3	87-010-237-910		CAP,E 1000UF-16V
CV6	87-015-681-080		CAP,E 10-16V
CV8	87-010-140-080		CAP,E 47-16V
CV10	SC-E10-86F-630		CAP,E 1000-16V
CV12	87-015-681-080		CAP,E 10-16V
CV13	87-015-684-080		CAP,E 47-16V
CV14	87-015-681-080		CAP,E 10-16V
CV15	87-015-681-080		CAP,E 10-16V
CV16	87-016-577-080		CAP,E 470UF-16V
CV21	87-010-060-080		CAP,E 100-16V
JACK1	S6-12H-K26-02A		TOTX178 TOSHIBA AN/DIP
JACK2	S5-720-75A-000		BJP-202L BAEEN BLACK
JACK3	S6-12R-IH0-05D		JACK,PPJ6031J
JACK4	S6-12R-BH0-08A		YKF51-5506 JALCO HORIZONT4P
JACK8			
KEY C.B			
SW508	S5-562-19B-000		SW,SKHV10910B
POWER C.B			
C900	87-010-408-040		CAP,E 47UF-50V
C901	S6-240-88B-000		CAP,0.1UF-250V
C902	S6-240-88B-000		CAP,0.1UF-250V
C902	S6-240-88F-000		CAP,PCX2 275V 0.1UF,M
C905	87-016-375-010		CAP,0.01UF-630V

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
C906	S6-240-87B-000		CAP,100P-1KV
C907	SA-1B3-0KH-2M0		CAP,220PF-400V
C913	87-012-379-010		CAP,3300PF-400V
C916	87-010-387-010		CAP,E 470UF-25V KME
C918	87-010-112-080		CAP,E 100-16V
C919	87-010-408-040		CAP,E 47UF-50V
C921	SC-E22-76F-638		CAP,E 220UF-16V
C923	87-010-237-910		CAP,E 1000UF-16V
C924	87-010-237-910		CAP,E 1000UF-16V
C925	87-010-375-080		CAP,E 330-10V
C926	87-010-408-040		CAP,E 47UF-50V
C927	87-015-684-080		CAP,E 47-16V
C929	87-010-112-080		CAP,E 100-16V
C932	SC-E47-7CD-638		CAP,E 470UF-10V
C934	SC-E47-7CD-638		CAP,E 470UF-10V
⚠F901	S5-850-11T-000		FUSE,1600MA 250V
⚠IC903	S6-570-62B-000		SENSOR PC123Y
⚠L901	S6-161-45H-000		FILTER SHT LFS2020V4-04350
⚠L901	S6-161-45J-000		FL BUJEON V-04350
L902	S6-330-88G-000		COIL,CHOCK TP 5MM
L903	S6-330-88D-000		COIL,20UH
R901	S6-140-07R-000		RES,2.7-2W
R902	SR-S10-03K-619		RES,100K-2W
R911	SR-S05-10K-619		RES,0.51-2W
R922	SR-S12-00J-619		RES,M/F 120-1W
⚠T901	S6-420-23T-000		PT,SHT-023T/KSE-023T
⚠V901	S6-560-04F-000		SVR681D10A SAMYANG 680V

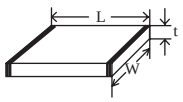
- Regarding connectors, they are not stocked as they are not the initial order items.
  The connectors are available after they are supplied from connector manufacturers upon the order is received.

○チップ抵抗部品コード／CHIP RESISTOR PART CODE

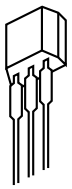
チップ抵抗部品コードの成り立ち
Chip Resistor Part Coding



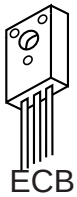
チップ抵抗
Chip resistor

容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm) 外形／Form	L	W	t	抵抗コード : A Resistor Code : A
1/16W	1005	±5%	CJ		1.0	0.5	0.35	104
1/16W	1608	±5%	CJ		1.6	0.8	0.45	108
1/10W	2125	±5%	CJ		2	1.25	0.45	118
1/8W	3216	±5%	CJ		3.2	1.6	0.55	128

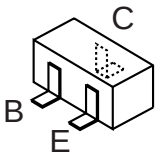
TRANSISTOR ILLUSTRATION



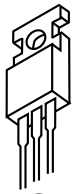
KRA105M
KRC105M
KRC103M



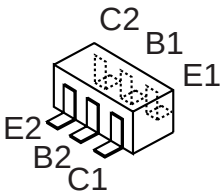
KSB1151



2SA1037K
KTA1504S
KTA1505S
KTC3198
KTC3875S
KTC4419
KTD1304S

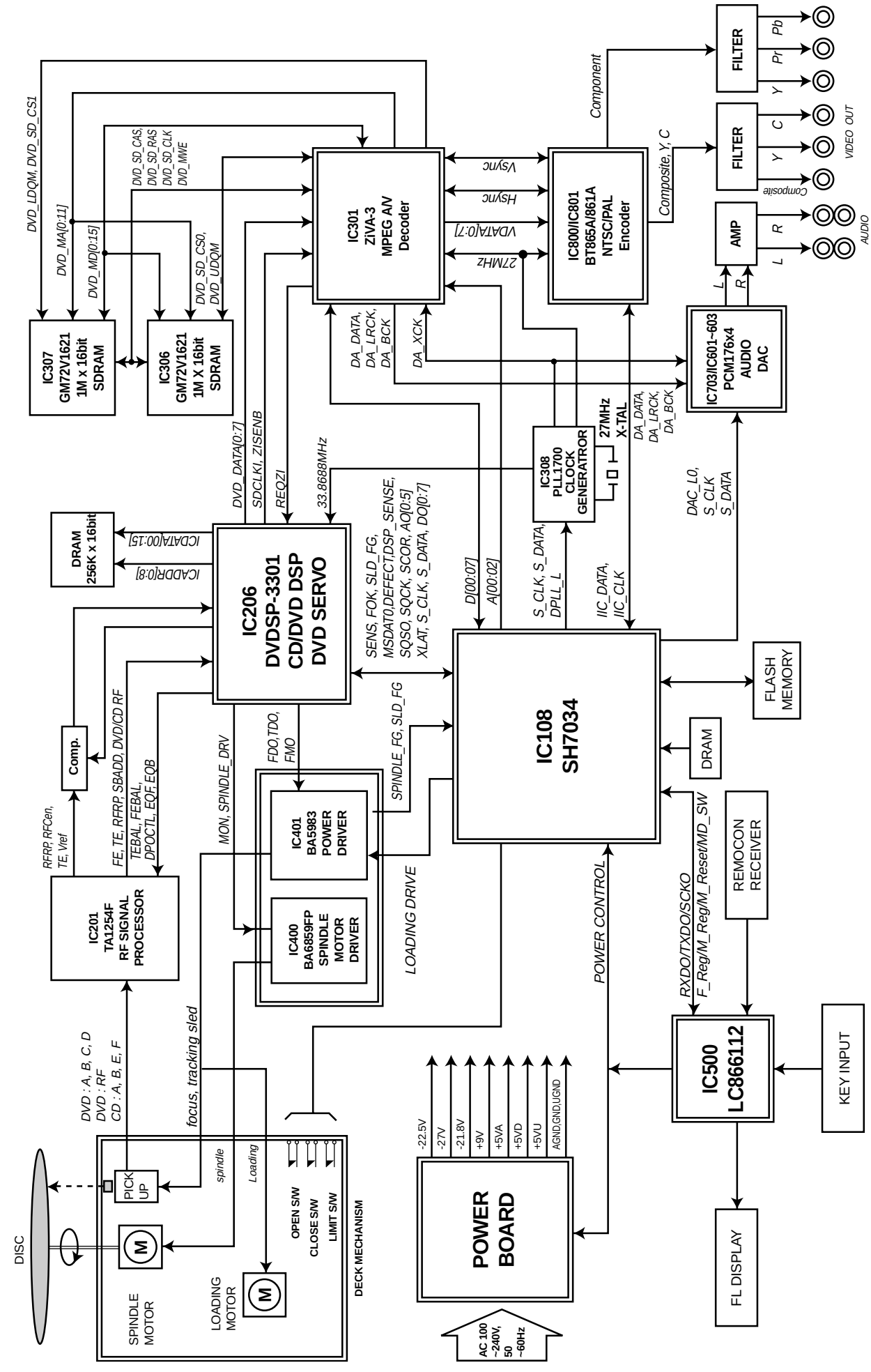


KSE13005F

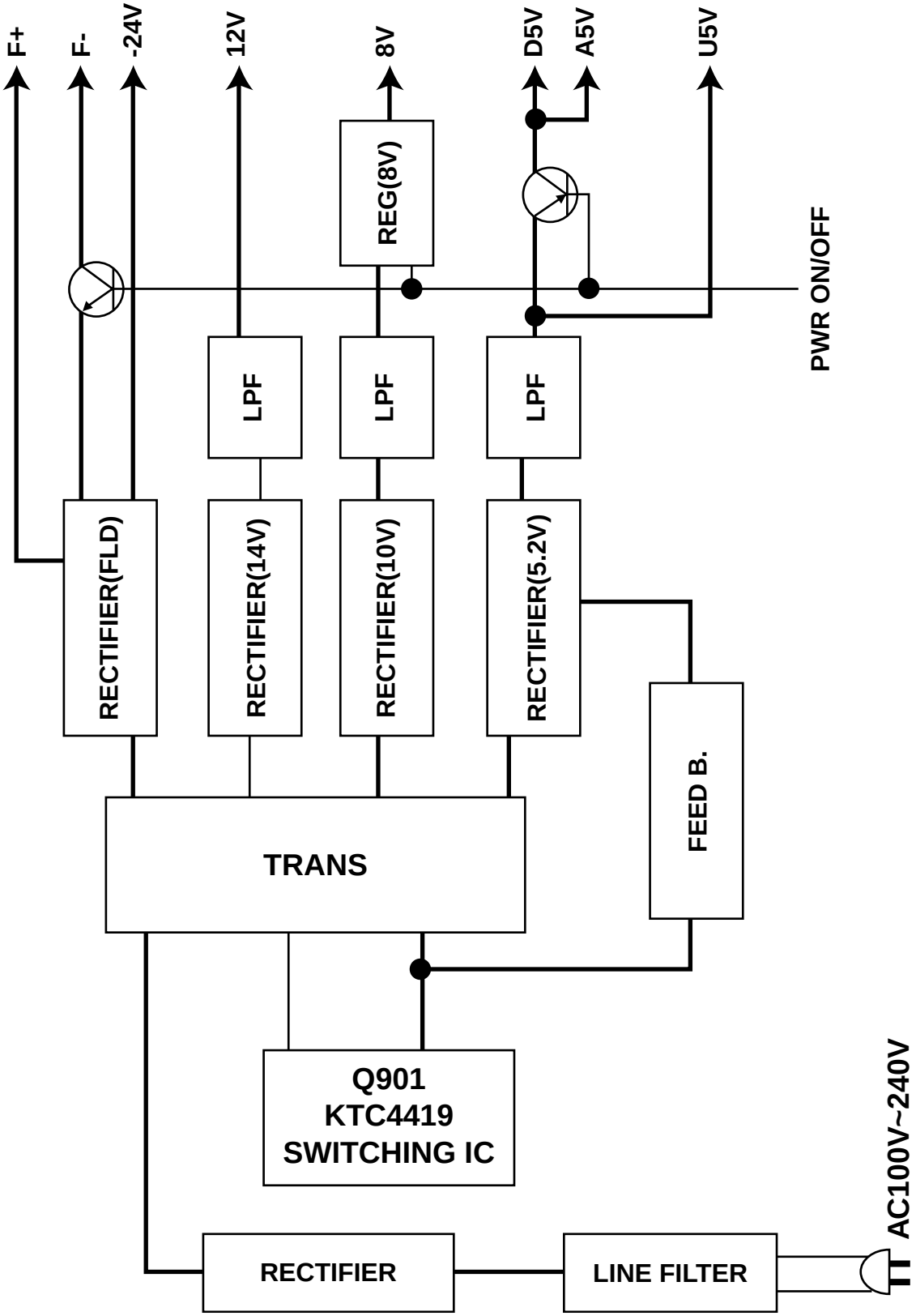


UMX1N
UMZ1N

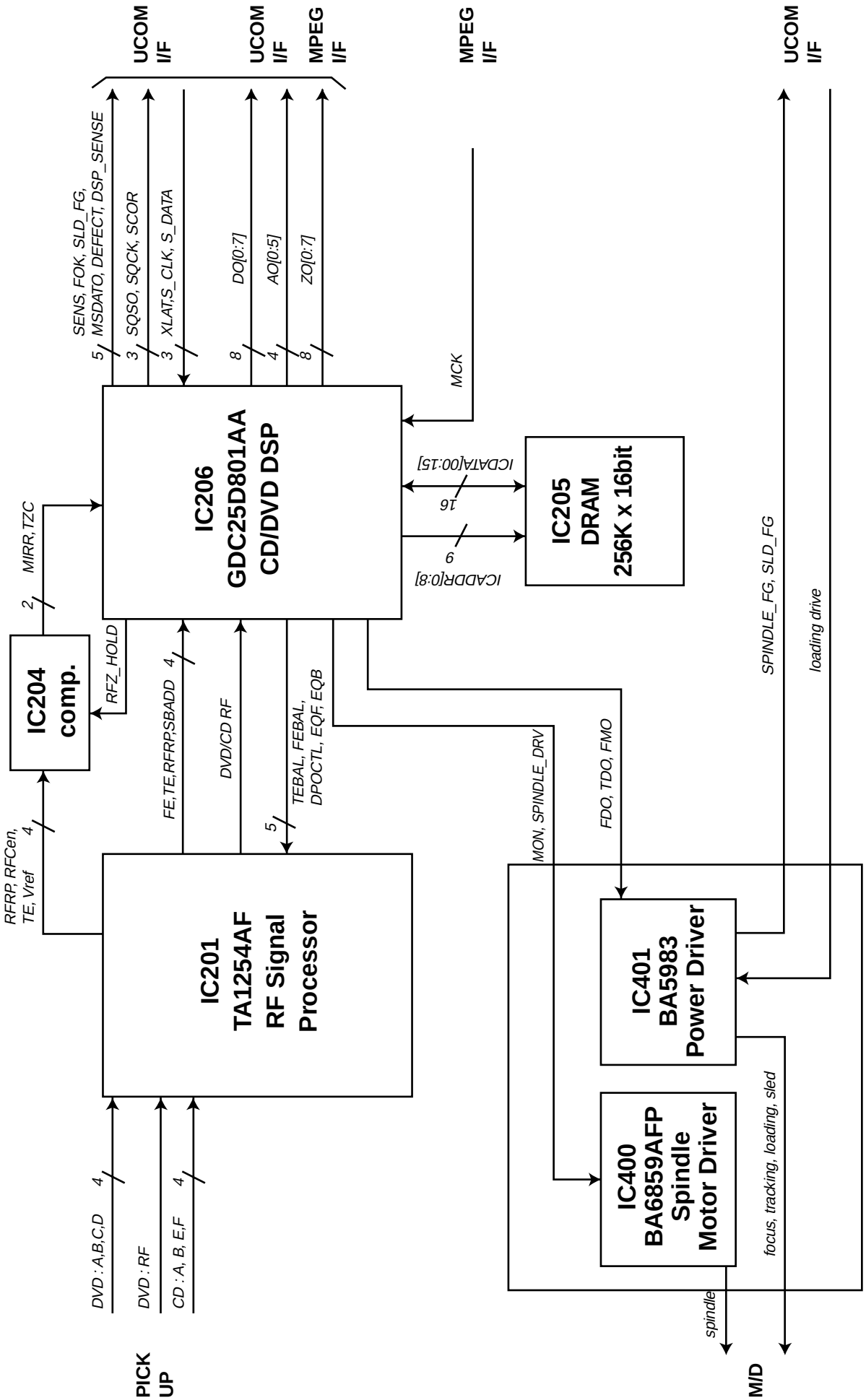
BLOCK DIAGRAM-1 (OVERALL)



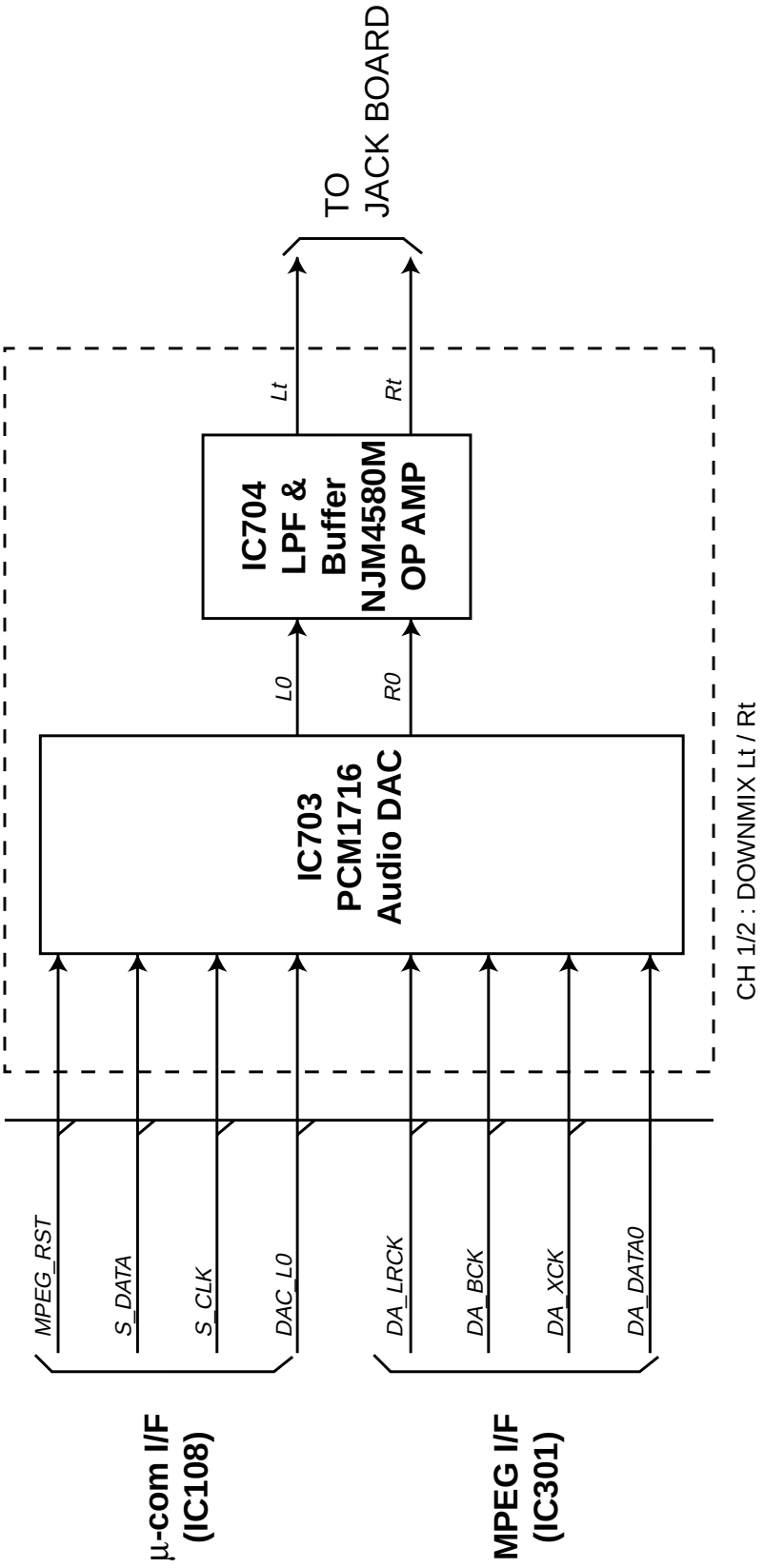
BLOCK DIAGRAM-2 (POWER)

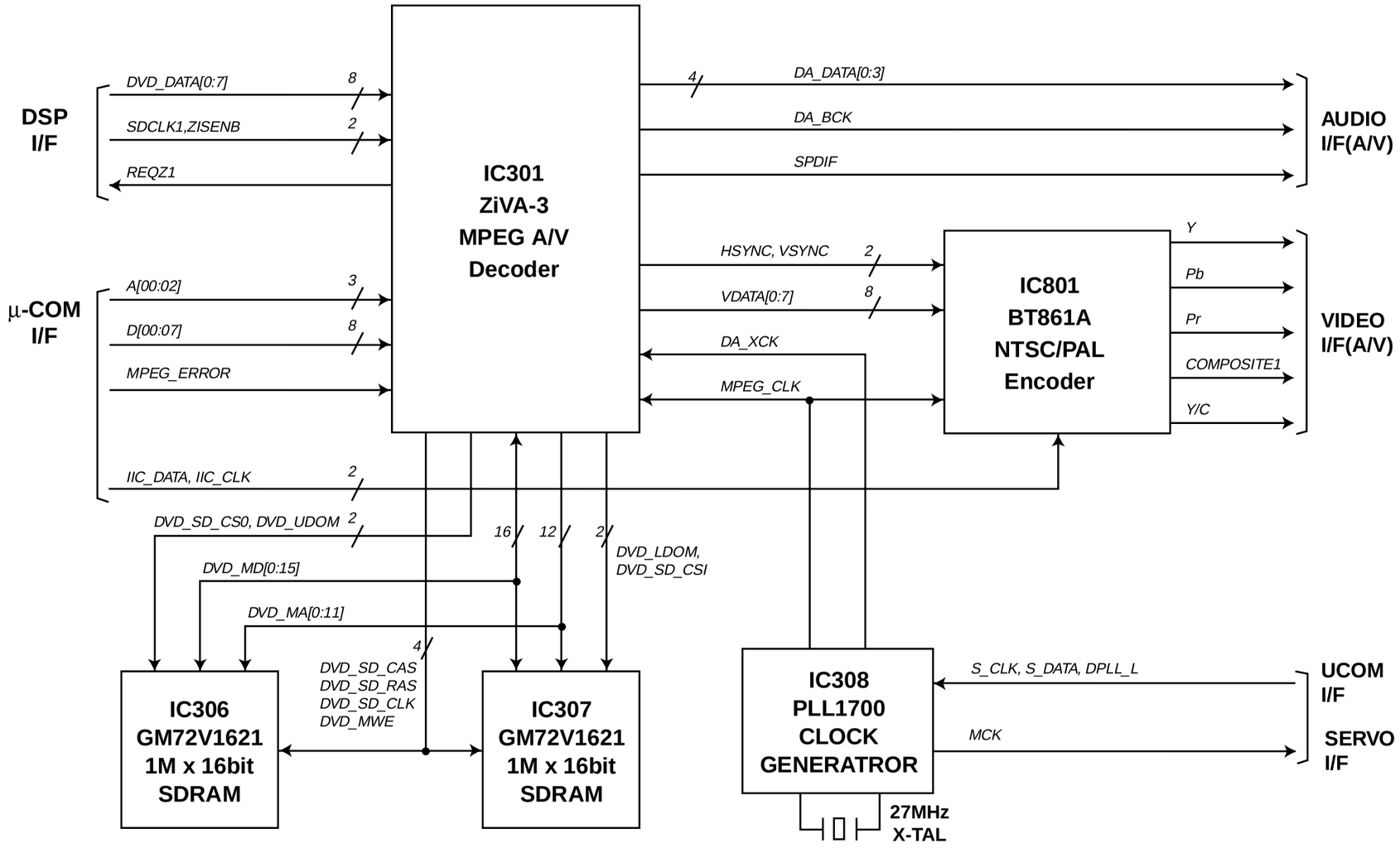


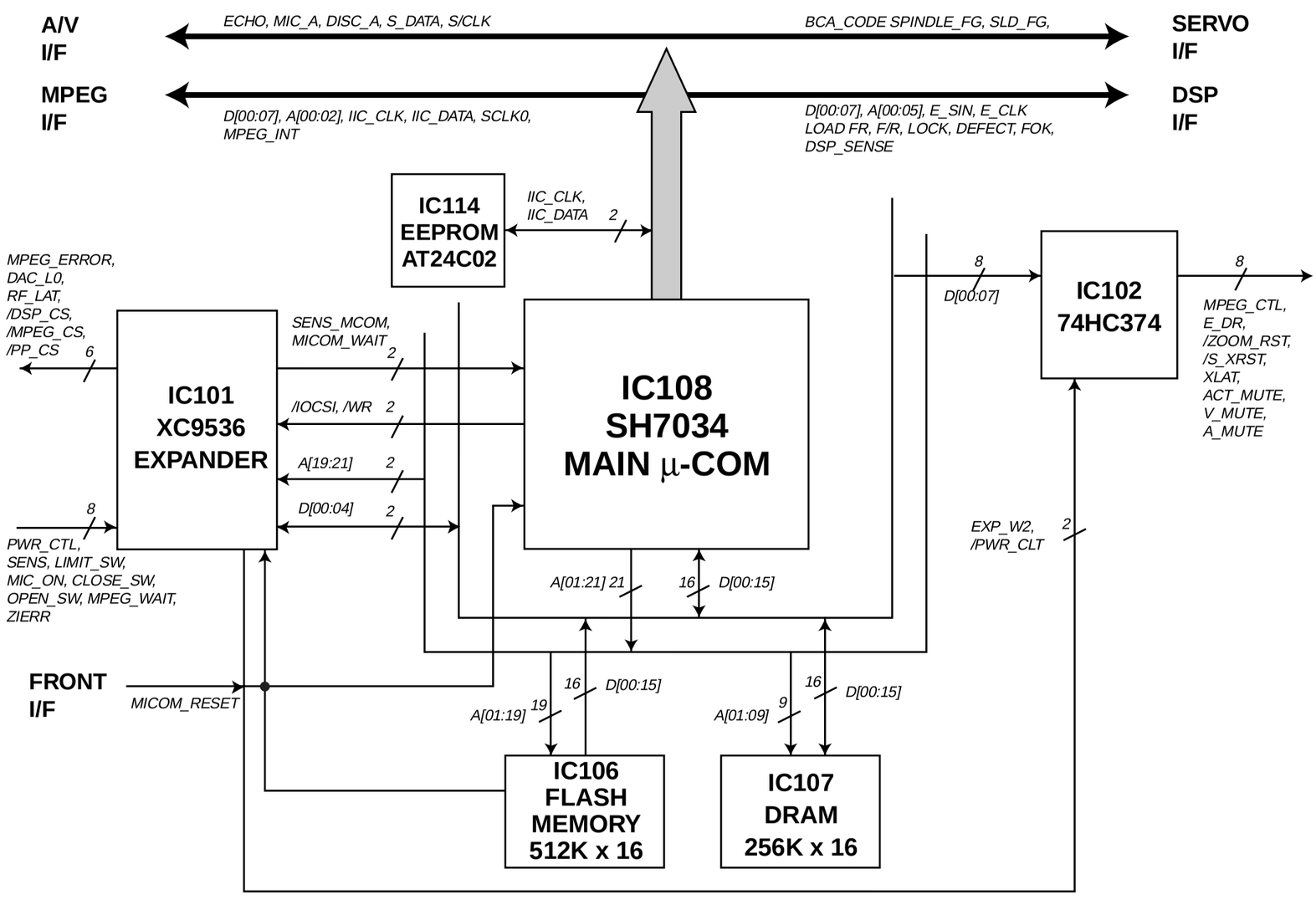
BLOCK DIAGRAM-3 (RF/DSP/SERVO)



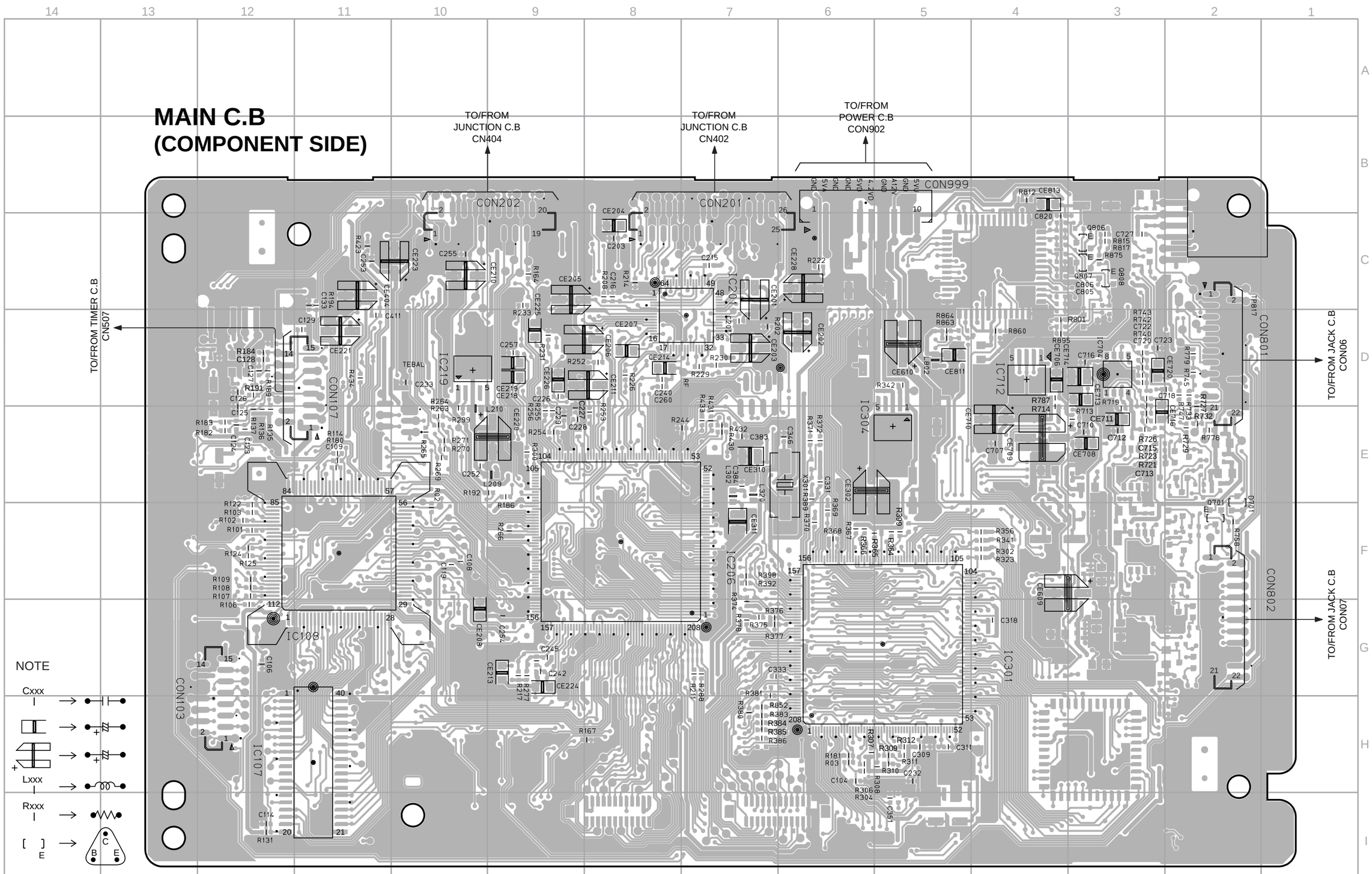
BLOCK DIAGRAM-4 (AUDIO)



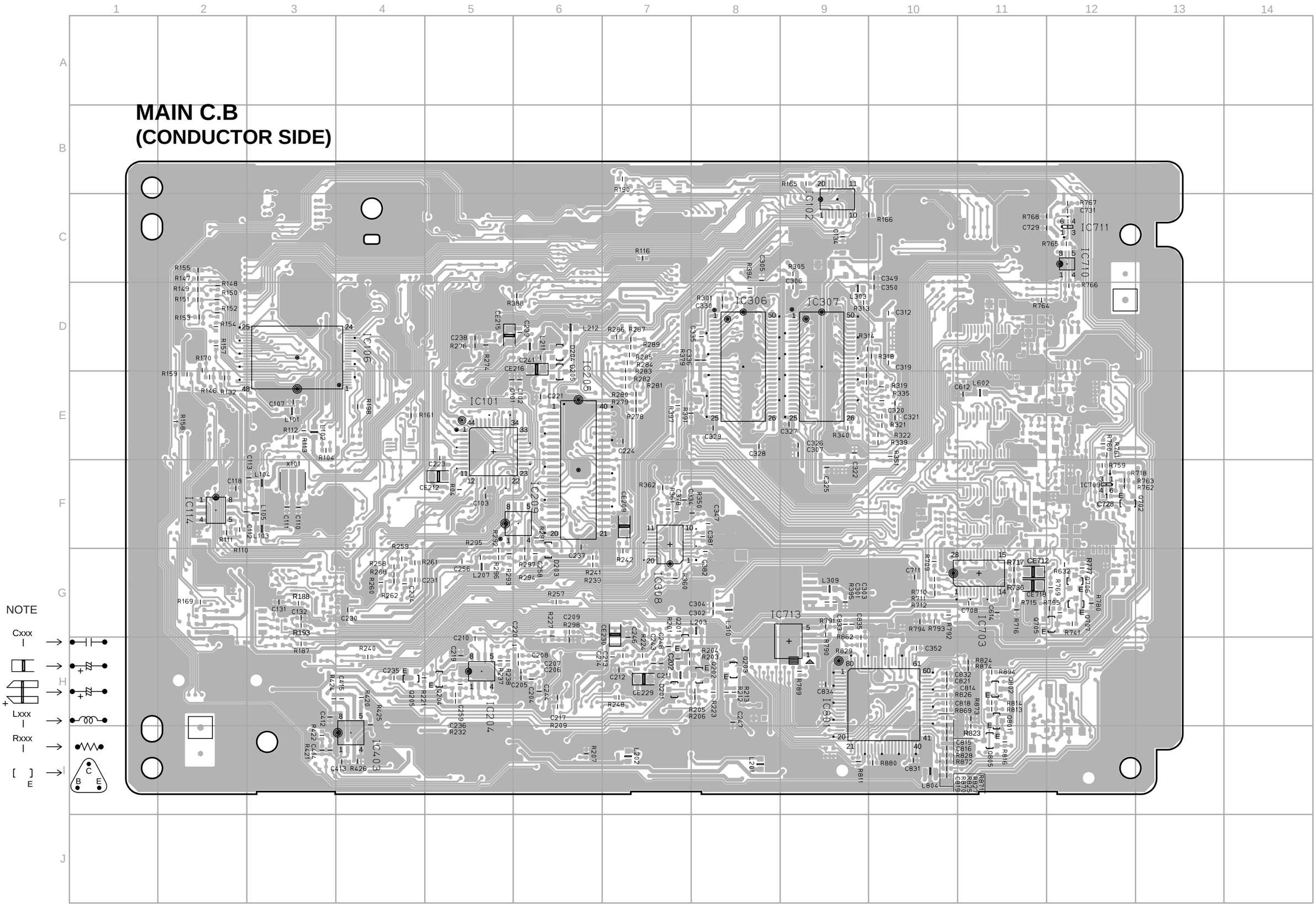

DSP I/F
DVD_DATA[0:7]
8
SDCLK1,ZISENB
2
REQZ1
μ-COM I/F
A[00:02]
3
D[00:07]
8
MPEG_ERROR
IIC_DATA, IIC_CLK
2
IC301
ZiVA-3
MPEG A/V
Decoder
4
DA_DATA[0:3]
DA_BCK
SPDIF
AUDIO I/F(A/V)
HSYNC, VSYNC
2
VDATA[0:7]
8
DA_XCK
MPEG_CLK
IC801
BT861A
NTSC/PAL
Encoder
Y
Pb
Pr
COMPOSITE1
Y/C
VIDEO I/F(A/V)
DVD_SD_CS0, DVD_UDOM
2
DVD_MD[0:15]
16
DVD_MA[0:11]
12
2
DVD_LDOM,
DVD_SD_CSI
4
DVD_SD_CAS
DVD_SD_RAS
DVD_SD_CLK
DVD_MWE
IC306
GM72V1621
1M x 16bit
SDRAM
IC307
GM72V1621
1M x 16bit
SDRAM
IC308
PLL1700
CLOCK
GENERATROR
27MHz
X-TAL
S_CLK, S_DATA, DPLL_L
MCK
UCOM I/F
SERVO I/F


A/V I/F
ECHO, MIC_A, DISC_A, S_DATA, S/CLK
BCA_CODE SPINDLE_FG, SLD_FG,
SERVO I/F
MPEG I/F
D[00:07], A[00:02], IIC_CLK, IIC_DATA, SCLK0,
MPEG_INT
D[00:07], A[00:05], E_SIN, E_CLK
LOAD FR, F/R, LOCK, DEFECT, FOK,
DSP_SENSE
DSP I/F
IC114
EEPROM
AT24C02
IIC_CLK,
IIC_DATA
2
MPEG_ERROR,
DAC_L0,
RF_LAT,
/DSP_CS,
/MPEG_CS,
/PP_CS
6
IC101
XC9536
EXPANDER
SENS_MCOM,
MICOM_WAIT
2
/IOCSI, /WR
2
A[19:21]
2
D[00:04]
2
8
PWR_CTL,
SENS, LIMIT_SW,
MIC_ON, CLOSE_SW,
OPEN_SW, MPEG_WAIT,
ZIERR
IC108
SH7034
MAIN μ-COM
A[01:21] 21
16
D[00:15]
8
D[00:07]
IC102
74HC374
8
MPEG_CTL,
E_DR,
/ZOOM_RST,
/S_XRST,
XLAT,
ACT_MUTE,
V_MUTE,
A_MUTE
EXP_W2,
/PWR_CLT
2
FRONT I/F
MICOM_RESET
16
D[00:15]
A[01:19]
19
16
D[00:15]
A[01:09]
9
IC106
FLASH
MEMORY
512K x 16
IC107
DRAM
256K x 16

MAIN C.B (COMPONENT SIDE)



MAIN C.B
(CONDUCTOR SIDE)



NOTE

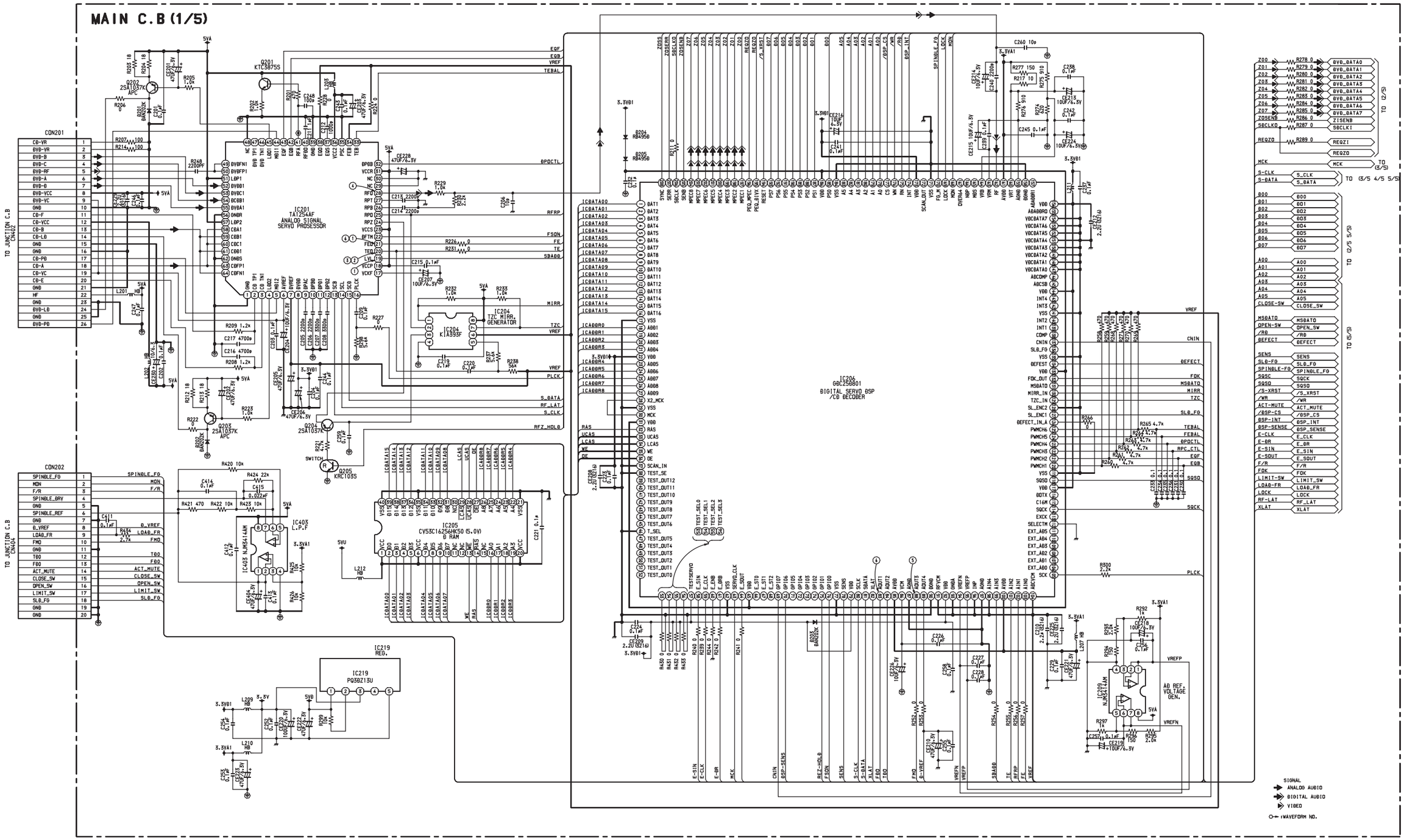
Cxxx

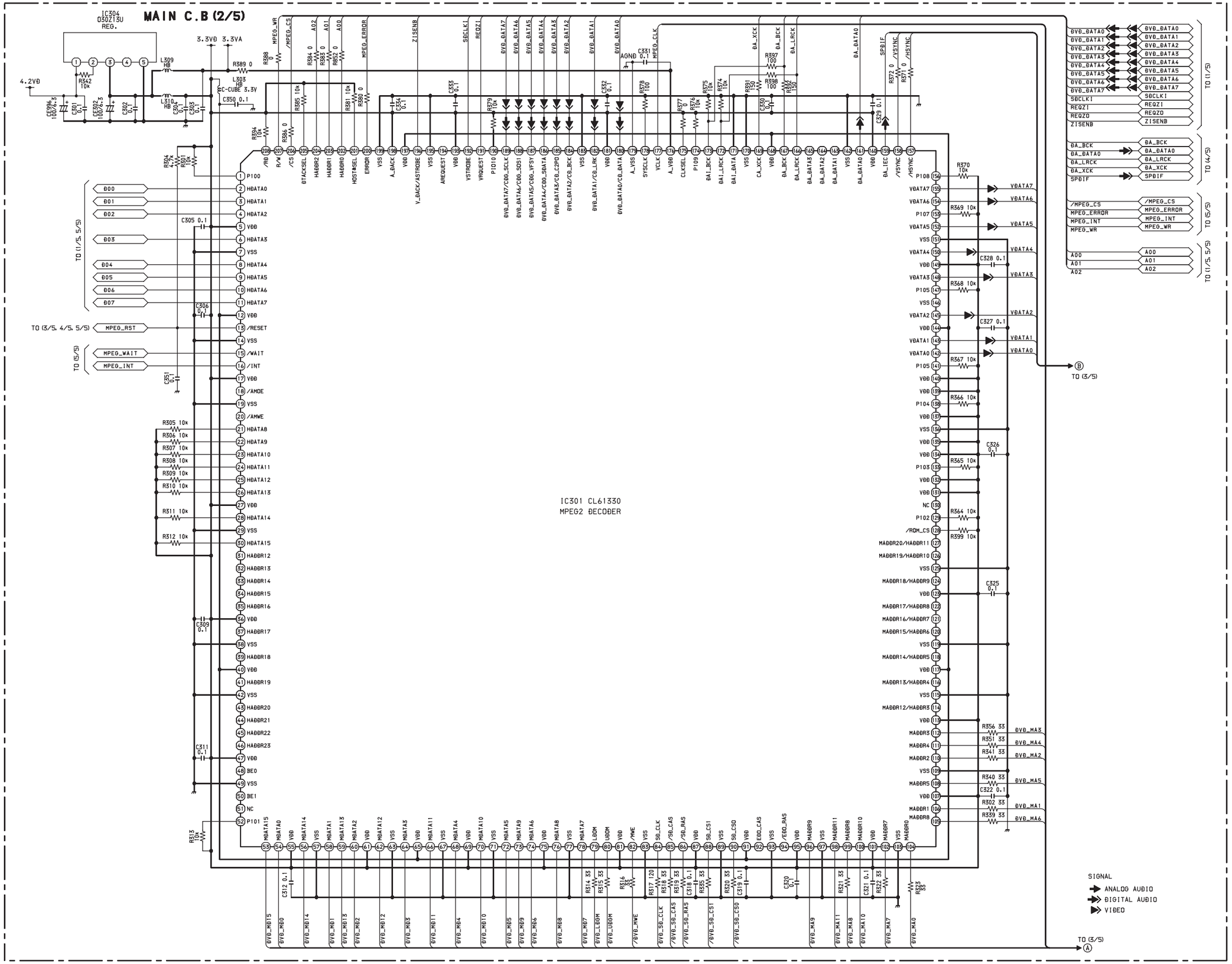
Lxxx

Rxxx

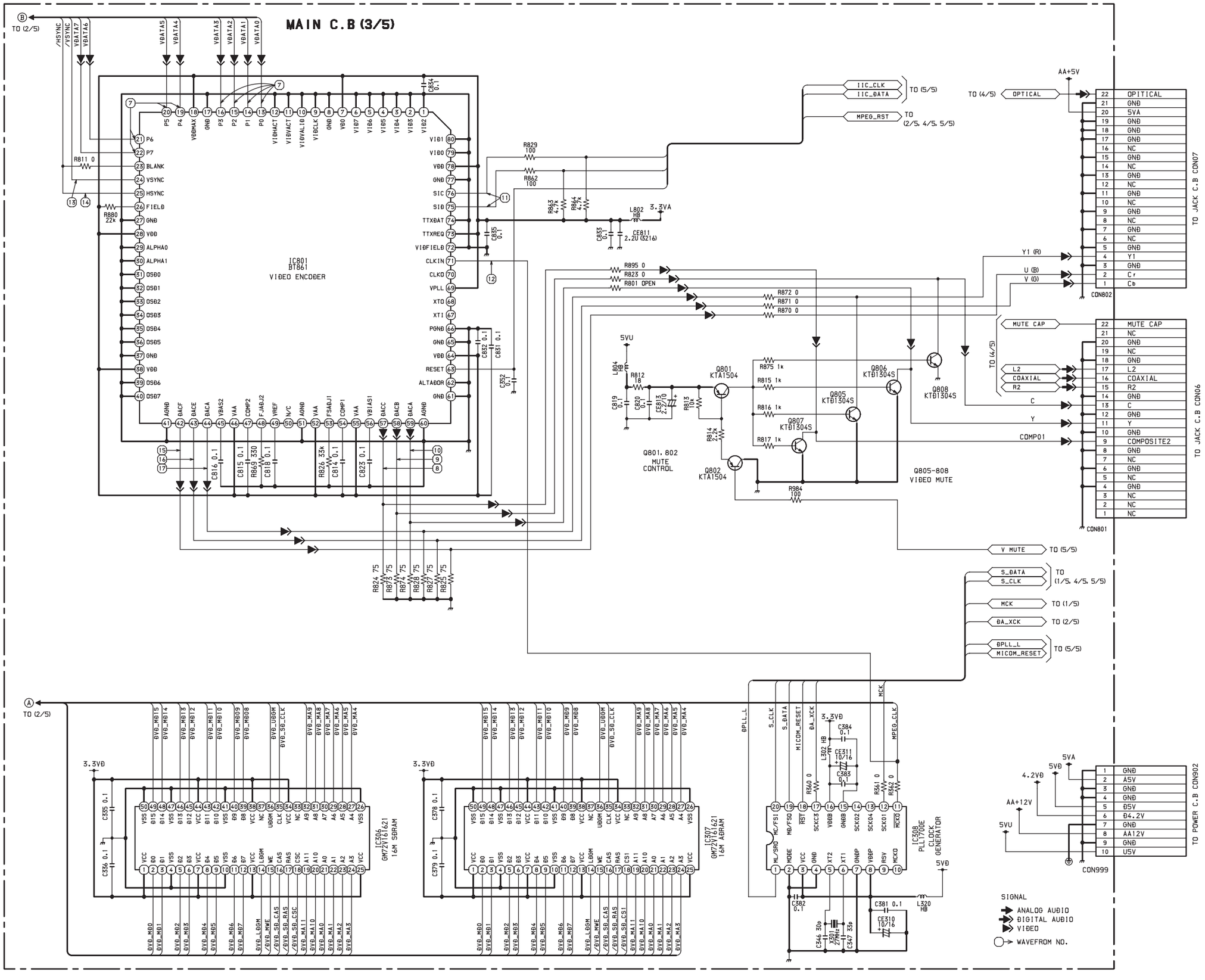
[ ]
E

SCHEMATIC DIAGRAM-1 (MAIN 1/5)

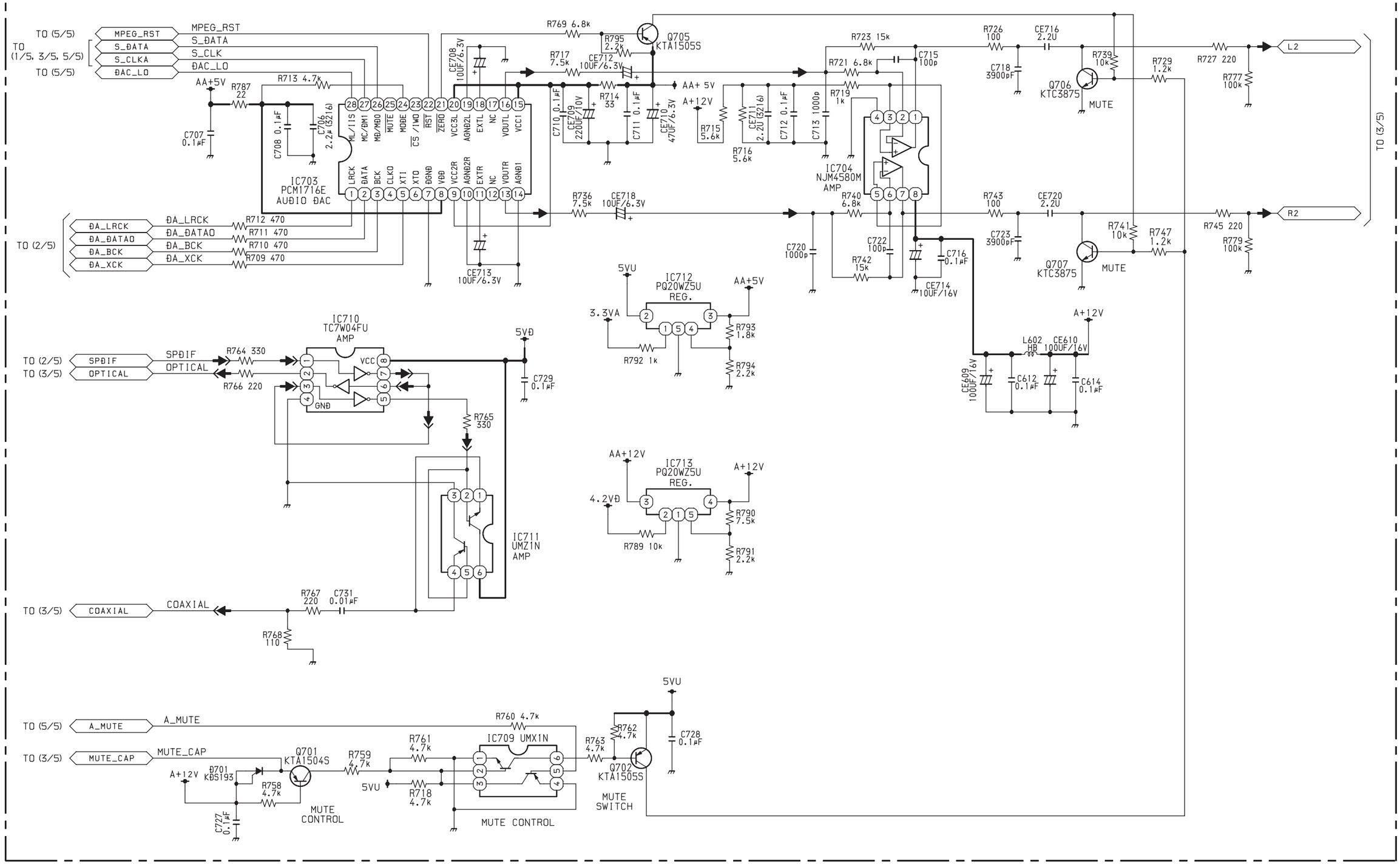



MAIN C.B (2/5)
IC304
D30713U
REG.
IC301 CL61330
MPEG2 DECODER
TO (1/5, 5/5)
TO (3/5, 4/5, 5/5)
TO (5/5)
TO (1/5)
TO (4/5)
TO (3/5)
TO (3/5)
SIGNAL
ANALOG AUDIO
DIGITAL AUDIO
VIDEO

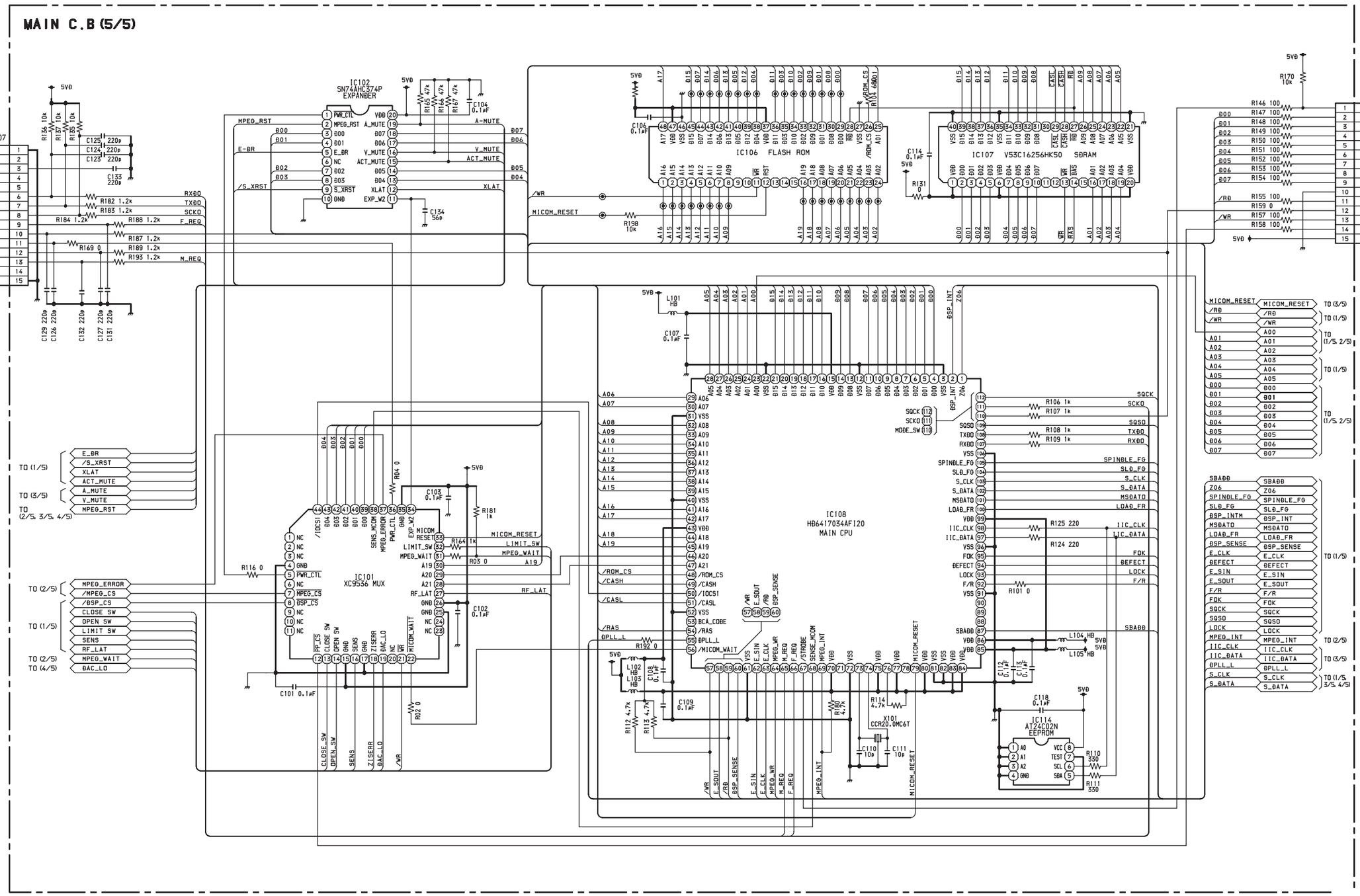
SCHEMATIC DIAGRAM-3 (MAIN 3/5)



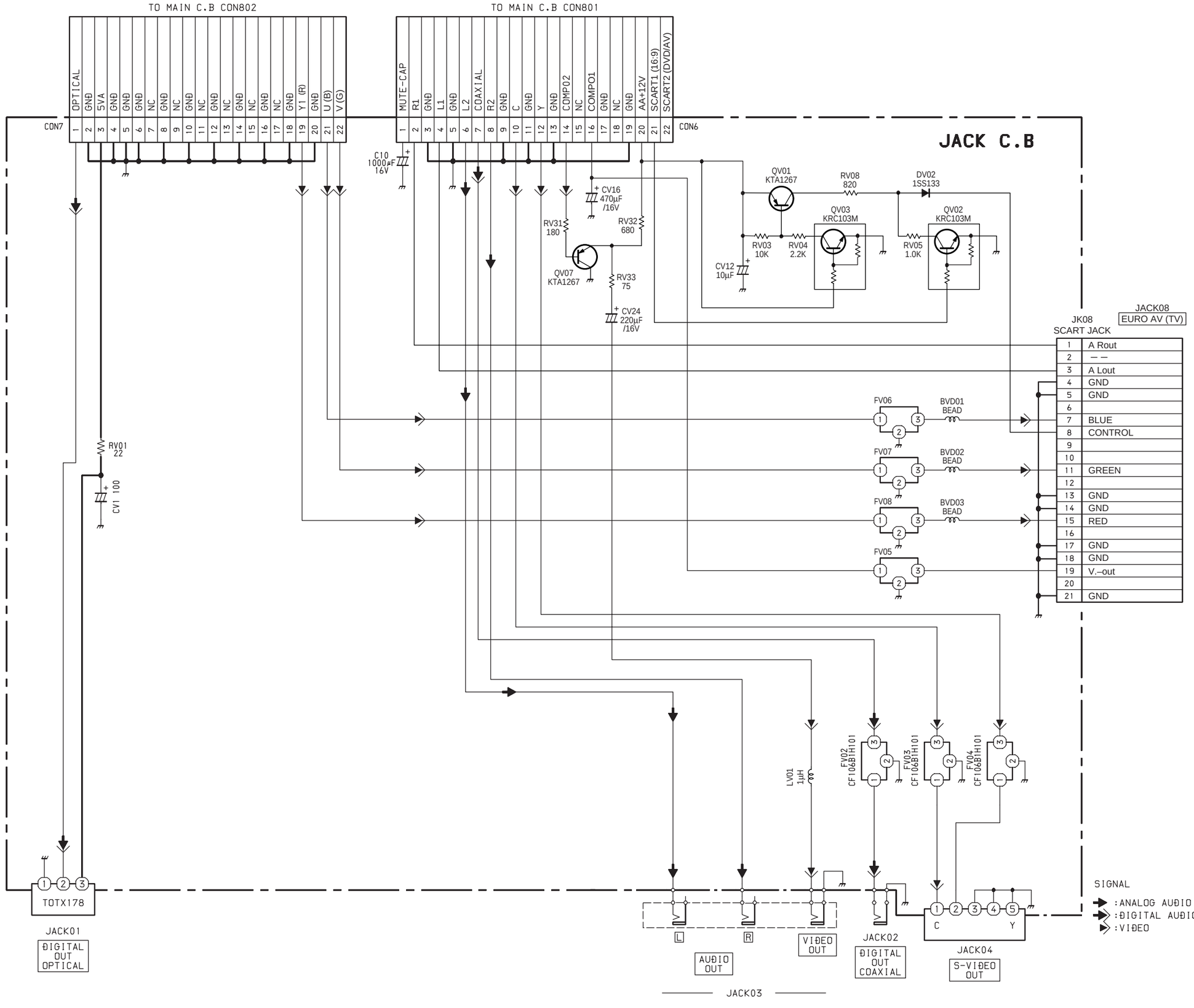
MAIN C.B (4/5)


TO (5/5)
MPEG_RST
S_DATA
S_CLK
DAC_LO
TO (1/5, 3/5, 5/5)
TO (5/5)
AA+5V
R787 22
C707 0.1μF
R713 4.7k
C708 0.1μF
C706 2.2μ (3216)
IC703
PCM1716E
AUDIO DAC
ML/IIS
MC/DMI
MD/MDO
MUTE
MODE
CS /IWO
RST
ZERO
VCC3L
AGND2L
EXTL
NC
VOUTL
VCC1
LRCK
DATA
BCK
CLKO
XTI
XTO
DGND
VDD
VCC2R
AGND2R
EXTR
NC
VOUTR
AGND1
TO (2/5)
DA_LRCK
DA_DATAO
DA_BCK
DA_XCK
R712 470
R711 470
R710 470
R709 470
CE713 10UF/6.3V
CE708 10UF/6.3V
R769 6.8k
R795 2.2k
Q705 KTA1505S
R717 7.5k
CE712 10UF/6.3V
AA+ 5V
A+12V
C710 0.1μF
CE709 220UF/10V
R714 33
C711 0.1μF
CE710 47UF/6.3V
R715 5.6k
R716 5.6k
CE711 2.2U (3216)
C712 0.1μF
C713 1000p
R723 15k
R721 6.8k
C715 100p
R719 1k
IC704
NJM4580M
AMP
R736 7.5k
CE718 10UF/6.3V
R740 6.8k
C720 1000p
C722 100p
R742 15k
C716 0.1μF
CE714 10UF/16V
R726 100
CE716 2.2U
C718 3900pF
Q706 KTC3875
MUTE
R739 10k
R729 1.2k
R727 220
R777 100k
L2
R743 100
CE720 2.2U
C723 3900pF
Q707 KTC3875
MUTE
R741 10k
R747 1.2k
R745 220
R779 100k
R2
TO (3/5)
5VU
IC712
PQ20WZ5U
REG.
3.3VA
AA+5V
R793 1.8k
R792 1k
R794 2.2k
A+12V
L602 HB
CE610 100UF/16V
CE609 100UF/16V
C612 0.1μF
C614 0.1μF
IC710
TC7W04FU
AMP
TO (2/5)
TO (3/5)
SPDIF
OPTICAL
R764 330
R766 220
VCC
GND
5VD
C729 0.1μF
R765 330
IC711
UMZ1N
AMP
AA+12V
IC713
PQ20WZ5U
REG.
A+12V
4.2VD
R789 10k
R790 7.5k
R791 2.2k
TO (3/5)
COAXIAL
R767 220
C731 0.01μF
R768 110
5VU
TO (5/5)
A_MUTE
TO (3/5)
MUTE_CAP
Q701 KTA1504S
D701 KDS193
A+12V
R758 4.7k
MUTE CONTROL
C727 0.1μF
R759 4.7k
5VU
R761 4.7k
R718 4.7k
R760 4.7k
IC709 UMX1N
MUTE CONTROL
R763 4.7k
R762 4.7k
C728 0.1μF
Q702 KTA1505S
MUTE SWITCH

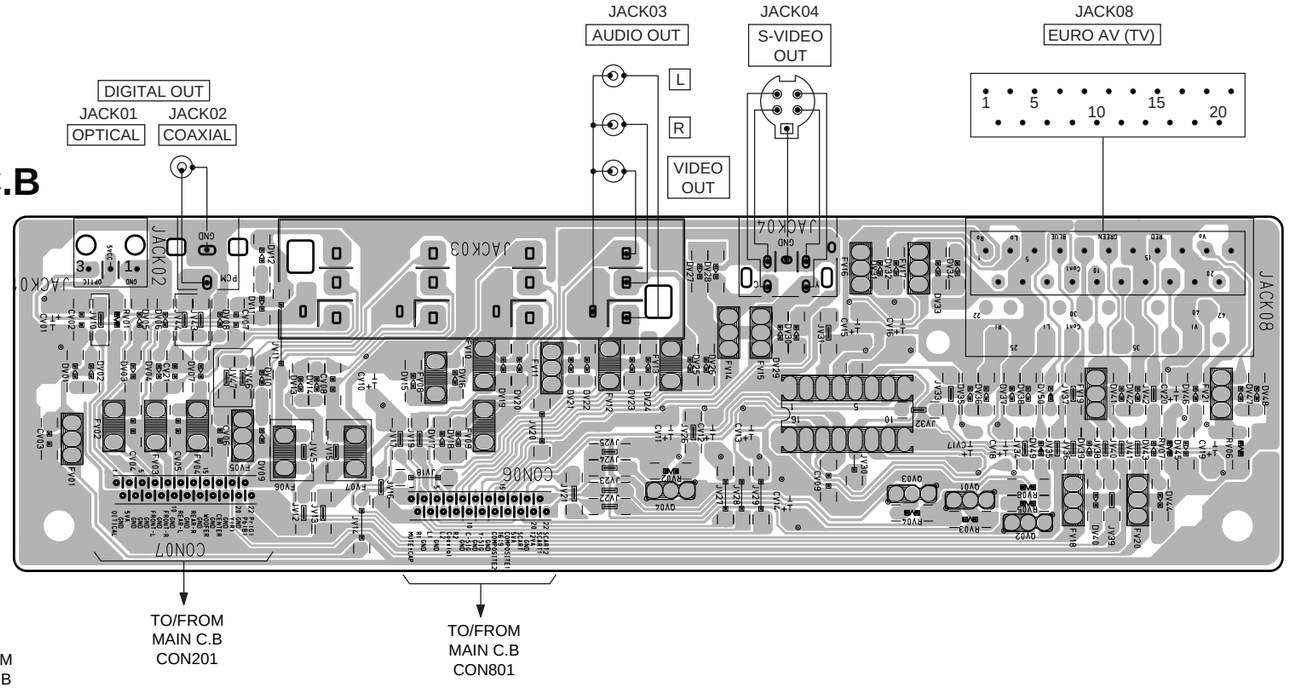
SCHEMATIC DIAGRAM-5 (MAIN 5/5)



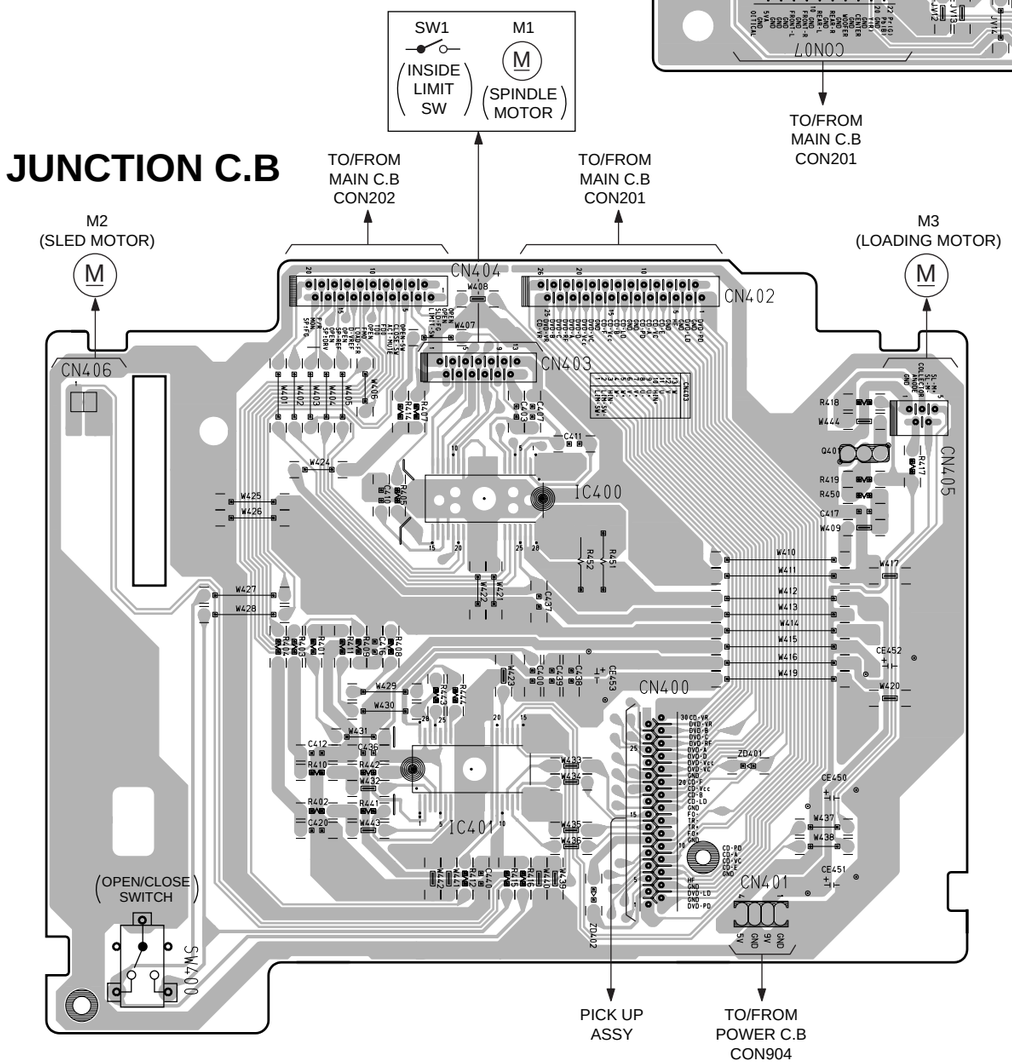
SCHEMATIC DIAGRAM-6 (JACK)



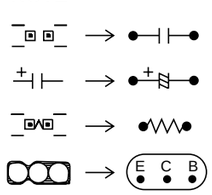
JACK C.B



JUNCTION C.B



NOTE



JUNCTION C.B

TO POWER C.B CON904

CN401

5V	4
GNĐ	3
9V	2
GNĐ	1

5V 9V

TO MAIN C.B CON201

CN402 GF102

CĐ-VR	26
ĐVĐ-VR	25
ĐVĐ-B	24
ĐVĐ-C	23
ĐVĐ-RF	22
ĐVĐ-A	21
ĐVĐ-Đ	20
ĐVĐ-VCC	19
ĐVĐ-VC	18
GNĐ	17
CĐ-F	16
CĐ-VCC	15
CĐ-B	14
CĐ-LĐ	13
GNĐ	12
GNĐ	11
CĐ-PĐ	10
CĐ-A	9
CĐ-VC	8
CĐ-E	7
GNĐ	6
HF	5
GNF	4
ĐVĐ-LĐ	3
GNĐ	2
ĐVĐ-PĐ	1

ZĐ401 MTZ10B

ZĐ402 MTZ10B

TO MAIN C.B CON202

CN404 GF102

SPINĐLE_FG	20
MON	19
F/R	18
SPINĐLE_ĐRV	17
OPEN	16
SPINĐLE_REF	15
OPEN	14
Đ_VREF	13
LOAĐ_FR	12
FMO	11
OPEN	10
TĐO	9
FĐO	8
ACT MUTE	7
CLOSE_SW	6
OPEN_SW	5
LIMIT_SW	4
SLĐ FG	3
OPEN	2
OPEN	1

IC400 BA6859AFP

1	N.C	RNF	28
2	A3	VM1	27
3	N.C	VM2	26
4	A2	VCC1	25
5	N.C	FG	24
6	N.C	PS	23
7	A1	EC	22
8	GNĐ	ECR	21
9	H1+	FR	20
10	H1-	N.C	19
11	H2+	SB	18
12	H2-	CNF	17
13	H3+	N.C	16
14	H3-	VH	15

C403 0.1μF, C407 0.1μF, C411 0.1μF, C437 0.1μF, C410 0.1μF

R451 1.0, R452 1.0, CE451 47/16V, CE450 47/16V, +9V, +5VA

R414 330, R405 150

W, V, U, U+, U-, V+, V-, W+, W-

SPINĐLE MOTOR ĐRIVE

SPINĐLE_FG, MON, SPINĐLE_ĐRV, SPINĐLE_REF, F/R

CN400

30	CĐ-VR
29	ĐVĐ-VR
28	ĐVĐ-B
27	ĐVĐ-C
26	ĐVĐ-RF
25	ĐVĐ-A
24	ĐVĐ-Đ
23	ĐVĐ-VCC
22	ĐVĐ-VC
21	GNĐ
20	CĐ-F
19	CĐ-VCC
18	CĐ-B
17	CĐ-LĐ
16	GNĐ
15	FO-
14	TR-
13	TR+
12	FO+
11	GNĐ
10	CĐ-PĐ
9	CĐ-A
8	CĐ-VC
7	CĐ-E
6	GNĐ
5	HF
4	GNĐ
3	ĐVĐ-LĐ
2	GNĐ
1	ĐVĐ-PĐ

OPTICAL PICKUP ASSY

IC401 BA5983FP

1	BIASIN	PreVcc	28
2	OPIN1 (+)	OPIN4 (+)	27
3	OPIN1 (-)	OPIN4 (-)	26
4	OPOUT1	OPOUT4	25
5	OPIN2 (+)	OPIN3 (+)	24
6	OPIN2 (-)	OPIN3 (-)	23
7	OPOUT2	OPOUT3	22
8	GNĐ	GNĐ	21
9	STBY1	STBY2	20
10	PowVcc1	PowVcc2	19
11	VO2 (-)	VO3 (-)	18
12	VO2 (+)	VO3 (+)	17
13	VO1 (-)	VO4 (-)	16
14	VO1 (+)	VO4 (+)	15

C436 0.1μF, C438 0.1μF, CE453 47/16V, C400 0.1μF, C416 0.1μF, C439 0.1μF, C435 47/16V, C440 0.1μF, C412 4700p, C420 8200p, CE452 47/16V

R403 1.0k, R410 33k, R404 1.0k, R402 20k, R442 20k, R441 20k, R411 10k, R401 4.7k, R443 5.6k, R408 10k, R409 1.0k, R444 8.2k, R412 10k

LOAĐ FR, FMO, FĐO, F_ACT-, F_ACT+, T_ACT-, T_ACT+

LOAĐING/SLEĐ MOTOR ĐRIVER

R419 4.7k, R450 1.0k, R418 6.8k, R416 10k, R415 10k, C417 0.047M

Q401 KRC103M SWITCH

SW400 MPU2016MLB (OPEN/CLOSE SW)

CN403 GF102

1	LIMIT_SW+
2	LIMIT_SW-
3	H1N-
4	W-
5	W+
6	V-
7	V+
8	U-
9	U+
10	H1N+
11	U
12	V
13	W

+5VA R407 10k

SW1 (INSIĐE LIMIT SWITCH)

M1 (SPINĐLE MOTOR)

CN405 GF102

1	GNĐ
2	ANOĐE
3	COLLECTOR
4	SL_M-
5	SL_M+

+5VA R417 120

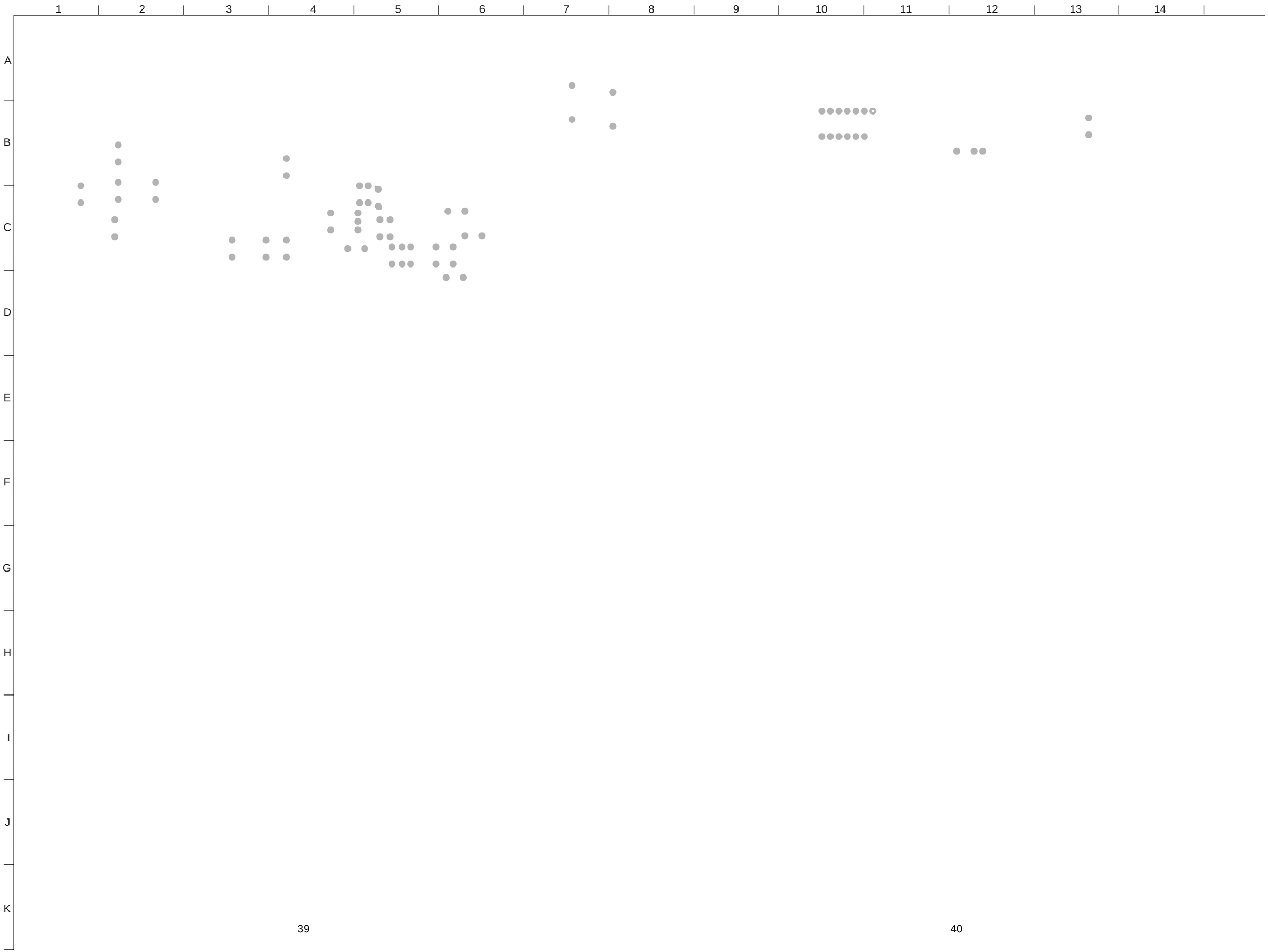
M2 (SLEĐ MOTOR)

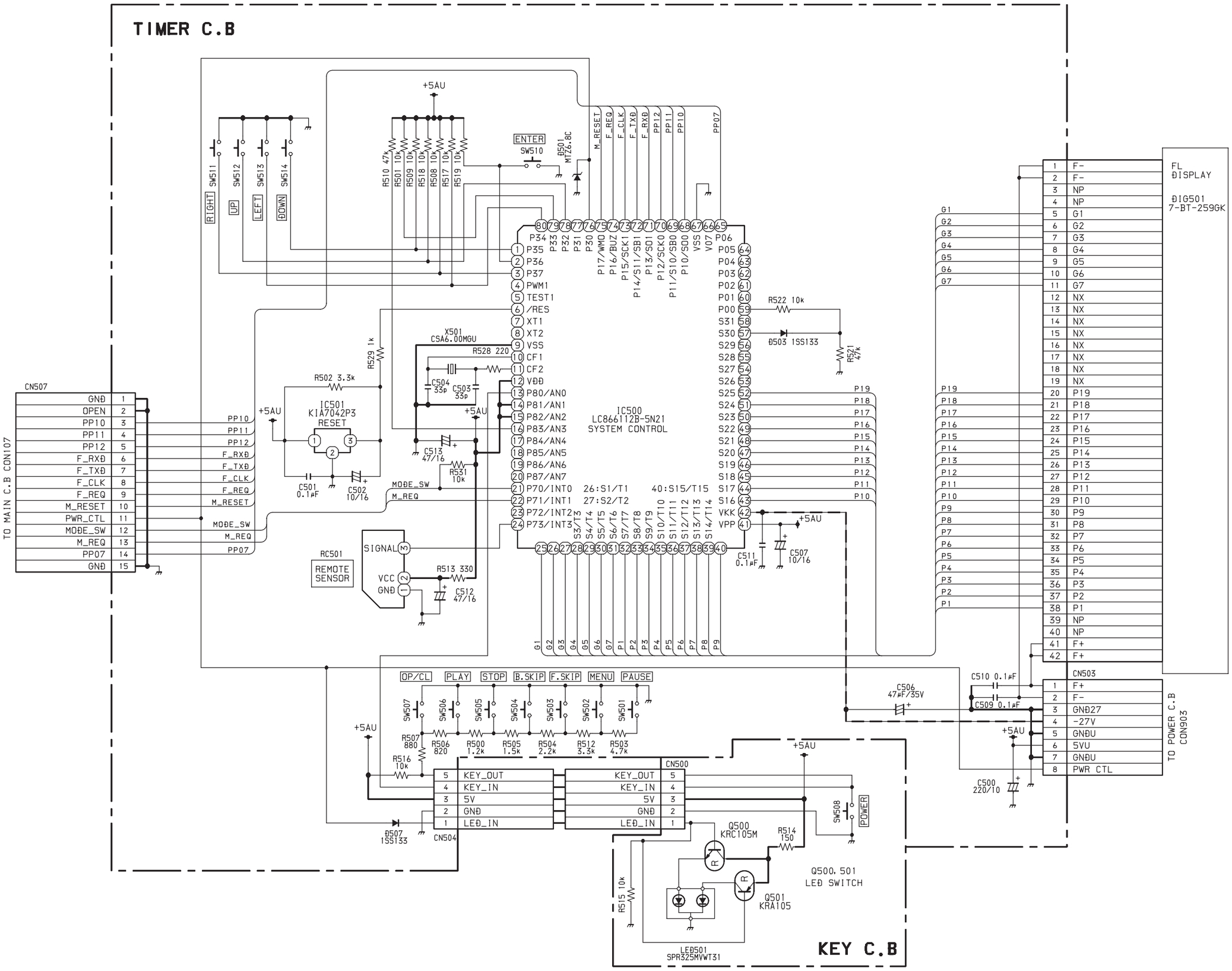
CN406 MA

1	LOAĐ_M-
2	LOAĐ_M+

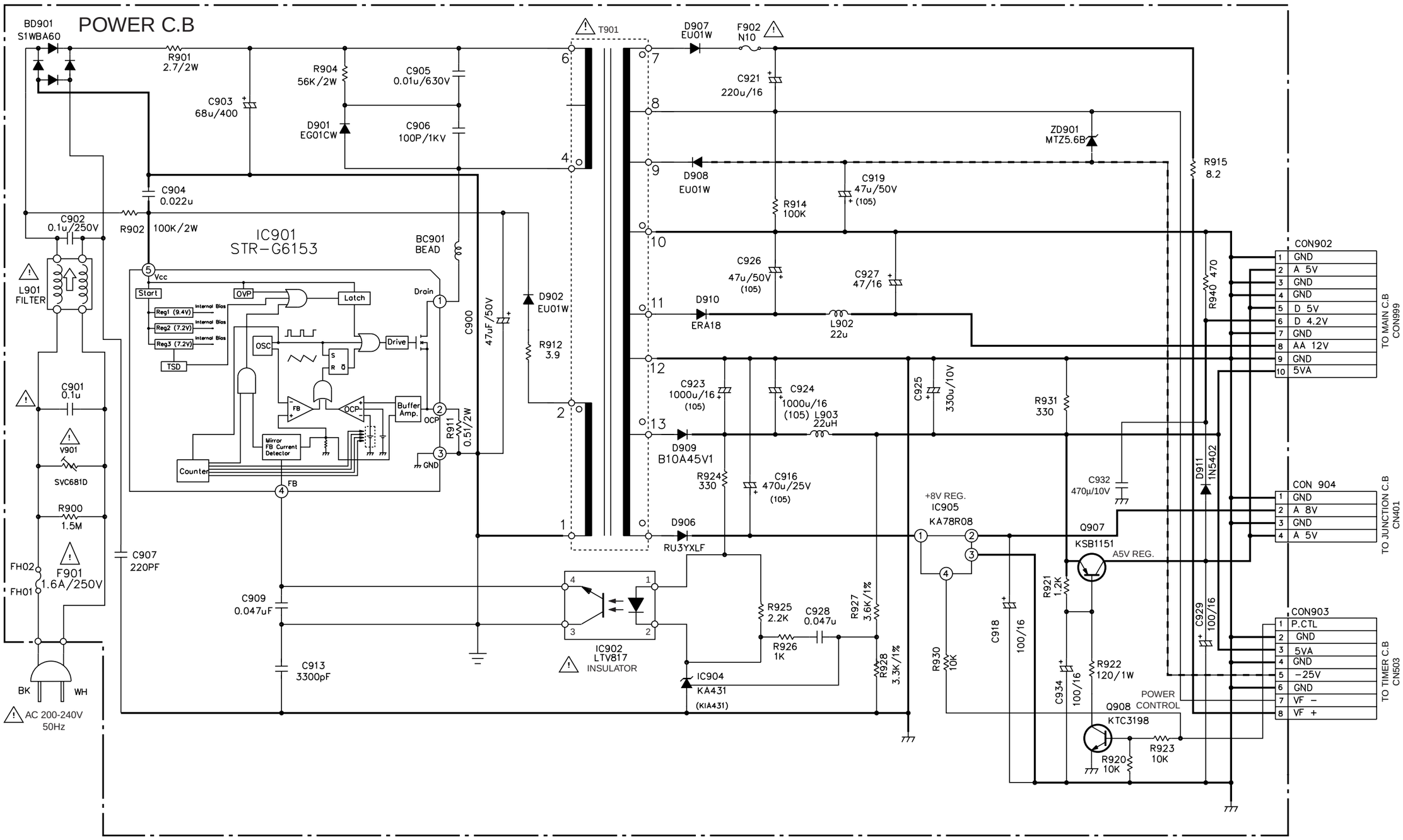
M3 (LOAĐING MOTOR)

WIRING-4 (TIMER/KEY/POWER)




TIMER C.B
TO MAIN C.B CON107
CN507
GNĐ 1
OPEN 2
PP10 3
PP11 4
PP12 5
F_RXĐ 6
F_TXĐ 7
F_CLK 8
F_REQ 9
M_RESET 10
PWR_CTL 11
MODE_SW 12
M_REQ 13
PP07 14
GNĐ 15
RIGHT SW511
UP SW512
LEFT SW513
DOWN SW514
ENTER SW510
Đ501 MTZ6.8C
R510 47k
R501 10k
R509 10k
R518 10k
R508 10k
R517 10k
R519 10k
+5AU
M_RESET
F_REQ
F_CLK
F_TXĐ
F_RXĐ
PP12
PP11
PP10
PP07
P34
P35
P36
P37
PWM1
TEST1
/RES
XT1
XT2
VSS
CF1
CF2
VĐĐ
P80/AN0
P81/AN1
P82/AN2
P83/AN3
P84/AN4
P85/AN5
P86/AN6
P87/AN7
P70/INT0
P71/INT1
P72/INT2
P73/INT3
P17/WMO
P16/BUZ
P15/SCK1
P14/S11/SB1
P13/SO1
P12/SCK0
P11/S10/SB0
P10/SO0
VSS
V07
P06
P05
P04
P03
P02
P01
P00
S31
S30
S29
S28
S27
S26
S25
S24
S23
S22
S21
S20
S19
S18
S17
S16
VKK
VPP
IC500
LC866112B-5N21
SYSTEM CONTROL
26:S1/T1
27:S2/T2
40:S15/T15
R522 10k
Đ503 1SS133
R521 47k
X501
CSA6.00MGU
R528 220
C504 33p
C503 33p
R529 1k
R502 3.3k
IC501
KIA7042P3
RESET
C501 0.1μF
C502 10/16
C513 47/16
R531 10k
MODE_SW
M_REQ
RC501
REMOTE SENSOR
SIGNAL
VCC
GNĐ
R513 330
C512 47/16
C511 0.1μF
C507 10/16
P19
P18
P17
P16
P15
P14
P13
P12
P11
P10
P9
P8
P7
P6
P5
P4
P3
P2
P1
G1
G2
G3
G4
G5
G6
G7
FL DISPLAY
ĐIG501
7-BT-259GK
1 F-
2 F-
3 NP
4 NP
5 G1
6 G2
7 G3
8 G4
9 G5
10 G6
11 G7
12 NX
13 NX
14 NX
15 NX
16 NX
17 NX
18 NX
19 NX
20 P19
21 P18
22 P17
23 P16
24 P15
25 P14
26 P13
27 P12
28 P11
29 P10
30 P9
31 P8
32 P7
33 P6
34 P5
35 P4
36 P3
37 P2
38 P1
39 NP
40 NP
41 F+
42 F+
C506 47μF/35V
C510 0.1μF
C509 0.1μF
C500 220/10
CN503
1 F+
2 F-
3 GNĐ27
4 -27V
5 GNĐU
6 5VU
7 GNĐU
8 PWR CTL
TO POWER C.B CON903
OP/CL SW507
PLAY SW506
STOP SW505
B.SKIP SW504
F.SKIP SW503
MENU SW502
PAUSE SW501
R507 880
R506 820
R500 1.2k
R505 1.5k
R504 2.2k
R512 3.3k
R503 4.7k
R516 10k
CN504
5 KEY_OUT
4 KEY_IN
3 5V
2 GNĐ
1 LEĐ_IN
CN500
Đ507 1SS133
Q500 KRC105M
R514 150
SW508 POWER
R515 10k
Q501 KRA105
Q500, 501
LEĐ SWITCH
LEĐ501 SPR325MVWT31
KEY C.B

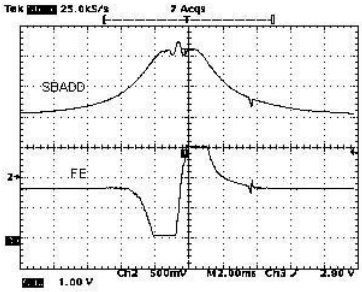
SCHEMATIC DIAGRAM-9 (POWER)



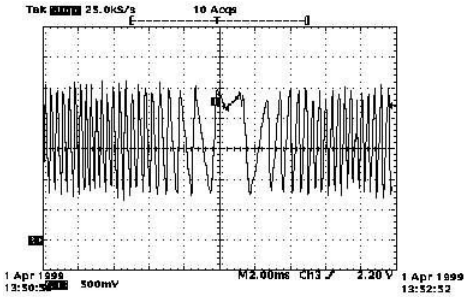
WAVE FORM

① IC201 Pin ⑲ (LVL) SBADD — VOLT/DIV: 500mV, TIME/DIV: 2mS

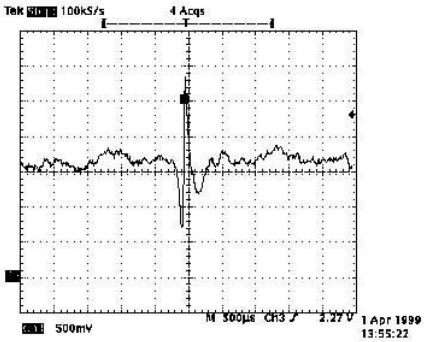
IC201 Pin ㉑ (FEO) Focus Error — VOLT/DIV: 2.9V, TIME/DIV: 2mS



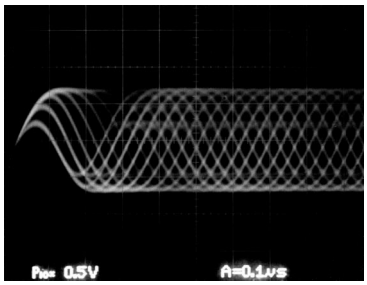
② IC201 Pin ⑳ (TEO) Tracking Error — VOLT/DIV: 2.2V, TIME/DIV: 2mS



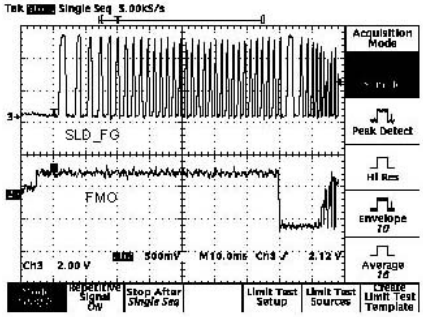
③ IC201 Pin ⑳ (TEO) VBR Tracking Error — VOLT/DIV: 2.27V, TIME/DIV: 500µS



④ IC201 Pin ㉘ (RFO) — VOLT/DIV: 0.5V, TIME/DIV: 0.1µS

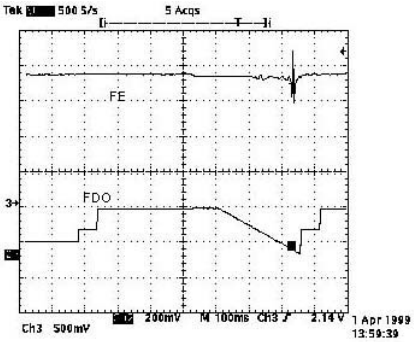


⑤ IC206 Pin ㊽ (A OUT3) SLED Drive (FMO) — VOLT/DIV: 2.12V, TIME/DIV: 10mS

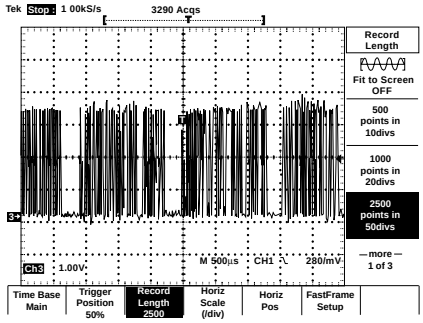


⑥ IC201 Pin ㉑ (FEO) Focus Error (In Focus search) — VOLT/DIV: 200mV, TIME/DIV: 100mS

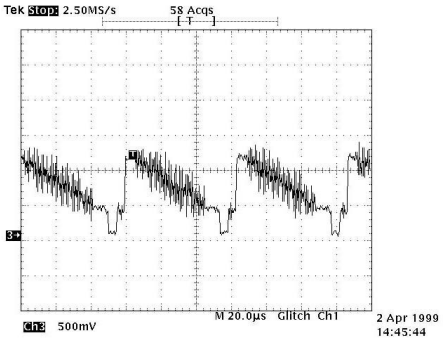
IC206 Pin ㉝ (A OUT1) Focus Drive (FDO) — VOLT/DIV: 2.14V, TIME/DIV: 100mS



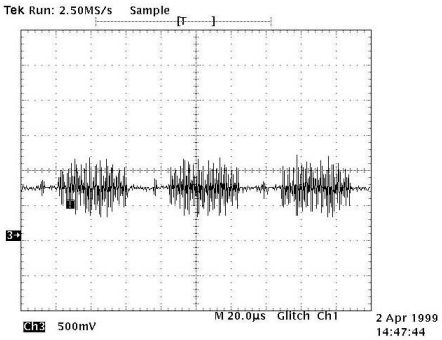
⑦ IC801 Pin ⑬-⑯ (P0-P3) IC801 Pin ⑲-㉒ (P4-P7) MPEG Data — VOLT/DIV: 280mV, TIME/DIV: 500µS



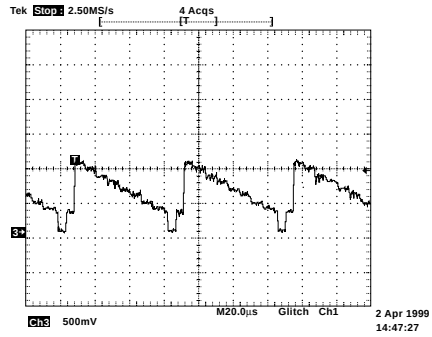
⑧ IC801 Pin ㊼ (DACC) VOLT/DIV: 500mV
Composite TIME/DIV: 20µS



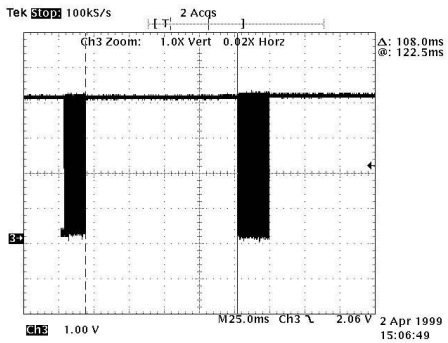
⑨ IC801 Pin ㊽ (DACB) VOLT/DIV: 500mV
Chrominance TIME/DIV: 20µS



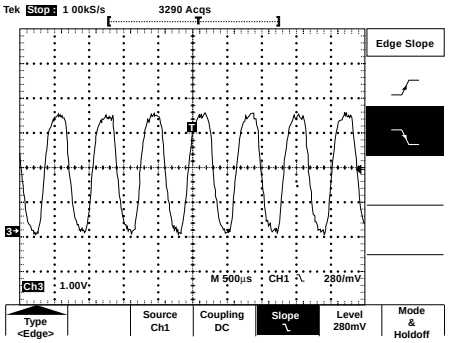
⑩ IC801 Pin ㊾ (DACA) VOLT/DIV: 500mV
Luminance TIME/DIV: 20µS



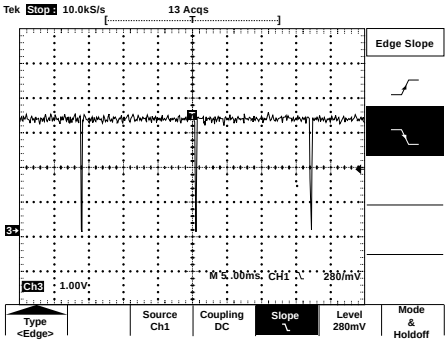
⑪ IC801 Pin ㉕ (SID) VOLT/DIV: 2.06V
IC801 Pin ㉖ (SIC) TIME/DIV: 25mS
SDA/SCL



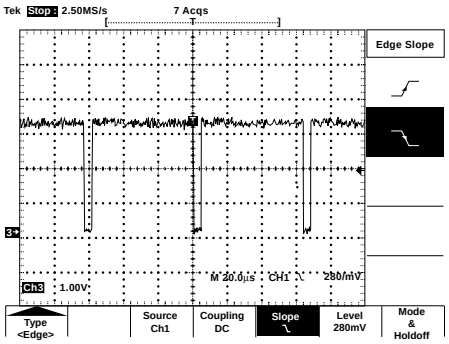
⑫ IC801 Pin ㉛ (CLK IN) VOLT/DIV: 280mV
MPEG Clock TIME/DIV: 500µS



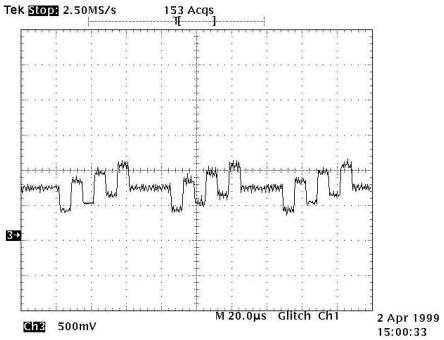
⑬ IC801 Pin ㉔ (VSYNC) VOLT/DIV: 280mV
Vertical SYNC TIME/DIV: 5mS



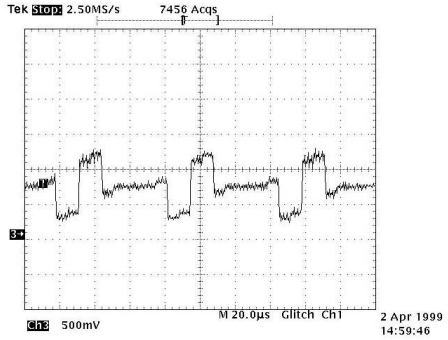
⑭ IC801 Pin ㉕ (HSYNC) VOLT/DIV: 280mV
TIME/DIV: 20µS



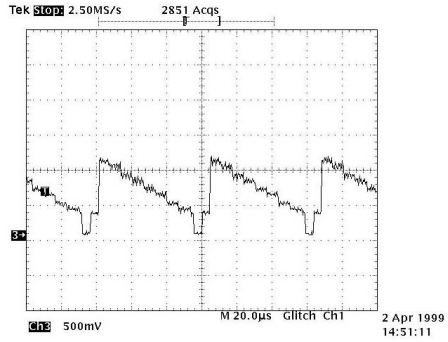
⑮ IC801 Pin ㊷ (DACF) VOLT/DIV: 500mV
Component Pb TIME/DIV: 20µS



⑯ IC801 Pin ㊸ (DACE) VOLT/DIV: 500mV
Component Pr TIME/DIV: 20µS



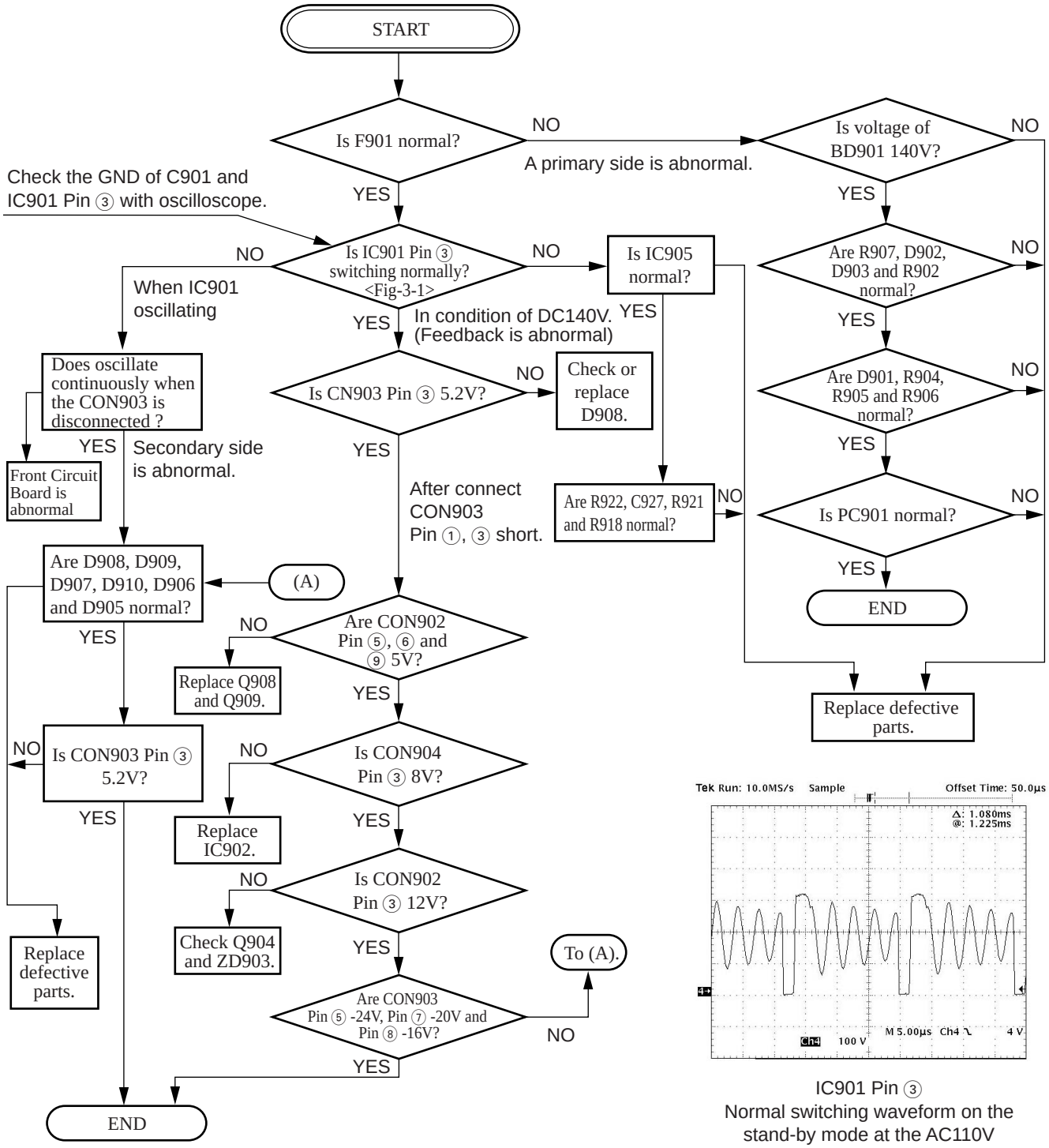
⑰ IC801 Pin ㊹ (DACA) VOLT/DIV: 500mV
Component Y TIME/DIV: 20µS



TROUBLE-SHOOTING

1. Power Circuit

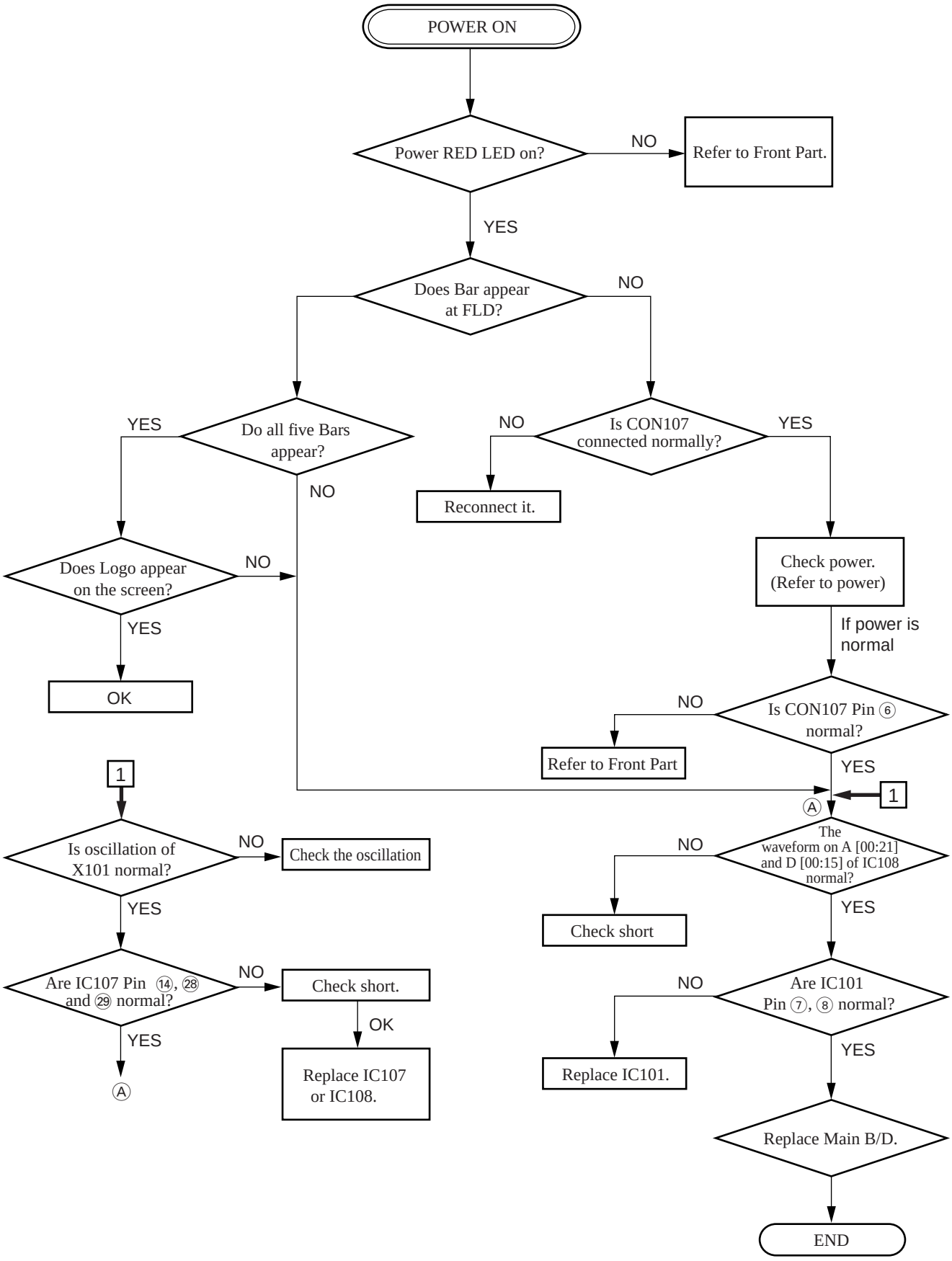
- Input Voltage: 120V
- It is possible to malfunction, if the unload condition is left for a long time when power is on.
  (More than Dummy load 100mA)
- A Primary side is abnormal when the fuse is short, secondary side is abnormal when the IC103 oscillates intermittently.
- The resistor value of both terminal is measured with DVM crossing each other to check the each element is normal or abnormal.
  (It is normal when the numerical value is different each other.)



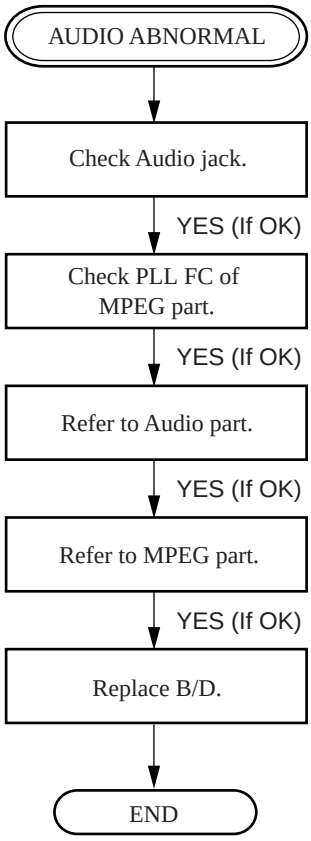
IC901 Pin ③
Normal switching waveform on the stand-by mode at the AC110V

2. µ-COM Circuit

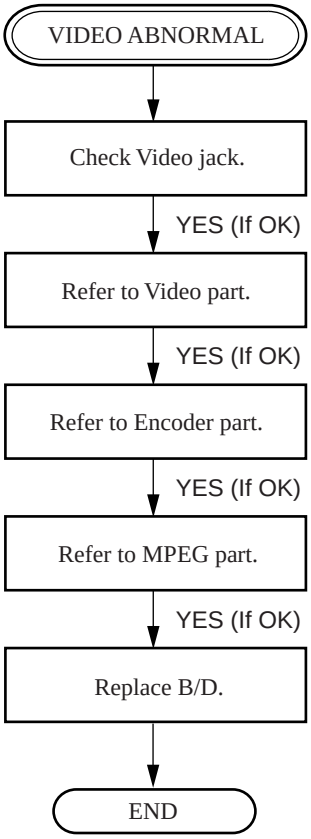
A. No Power



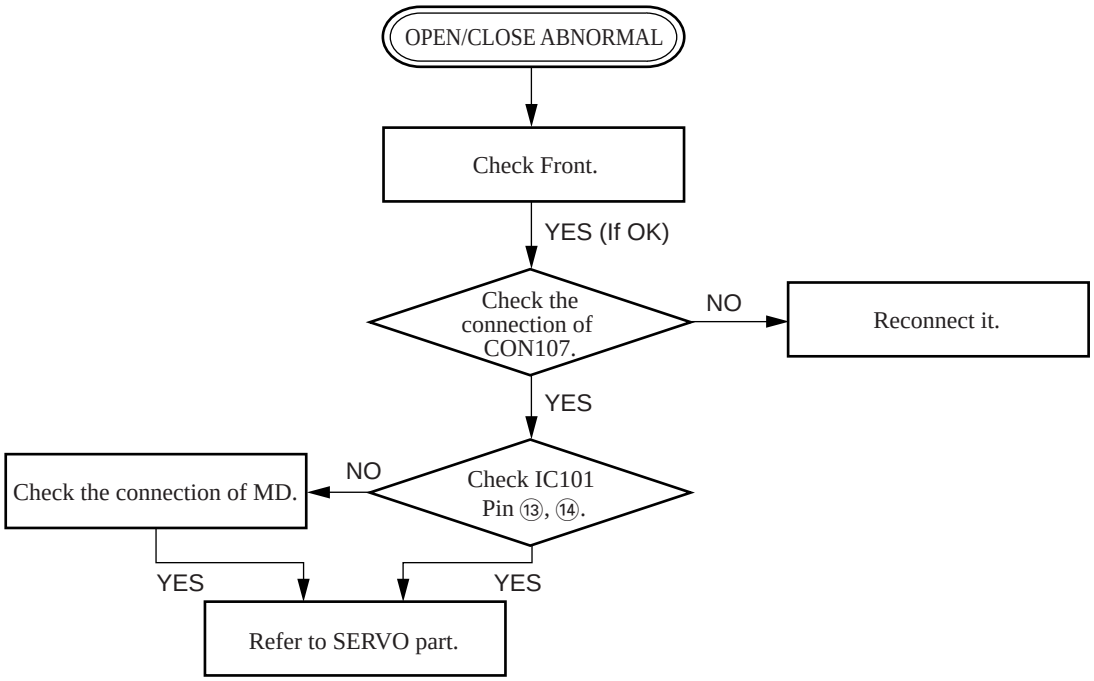
B. Audio abnormal



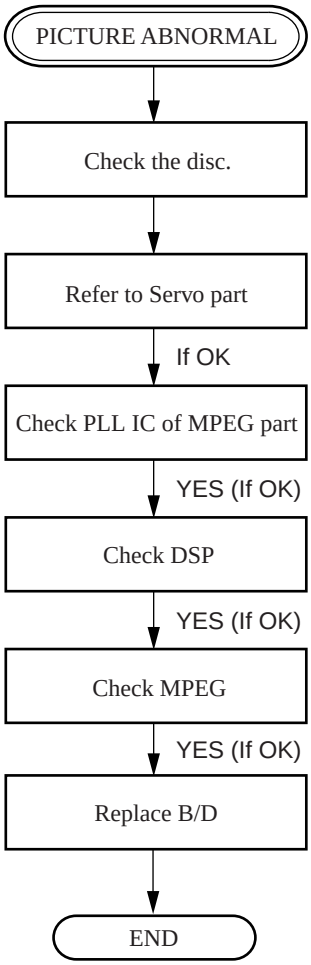
C. Video abnormal



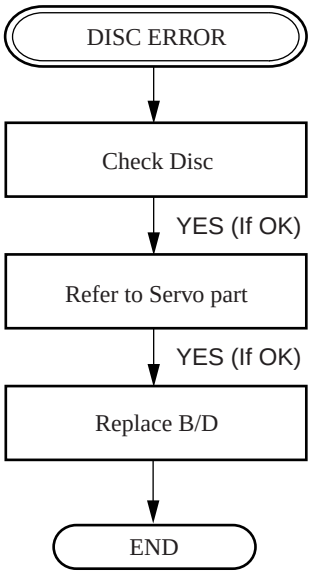
D. Open/Close abnormal



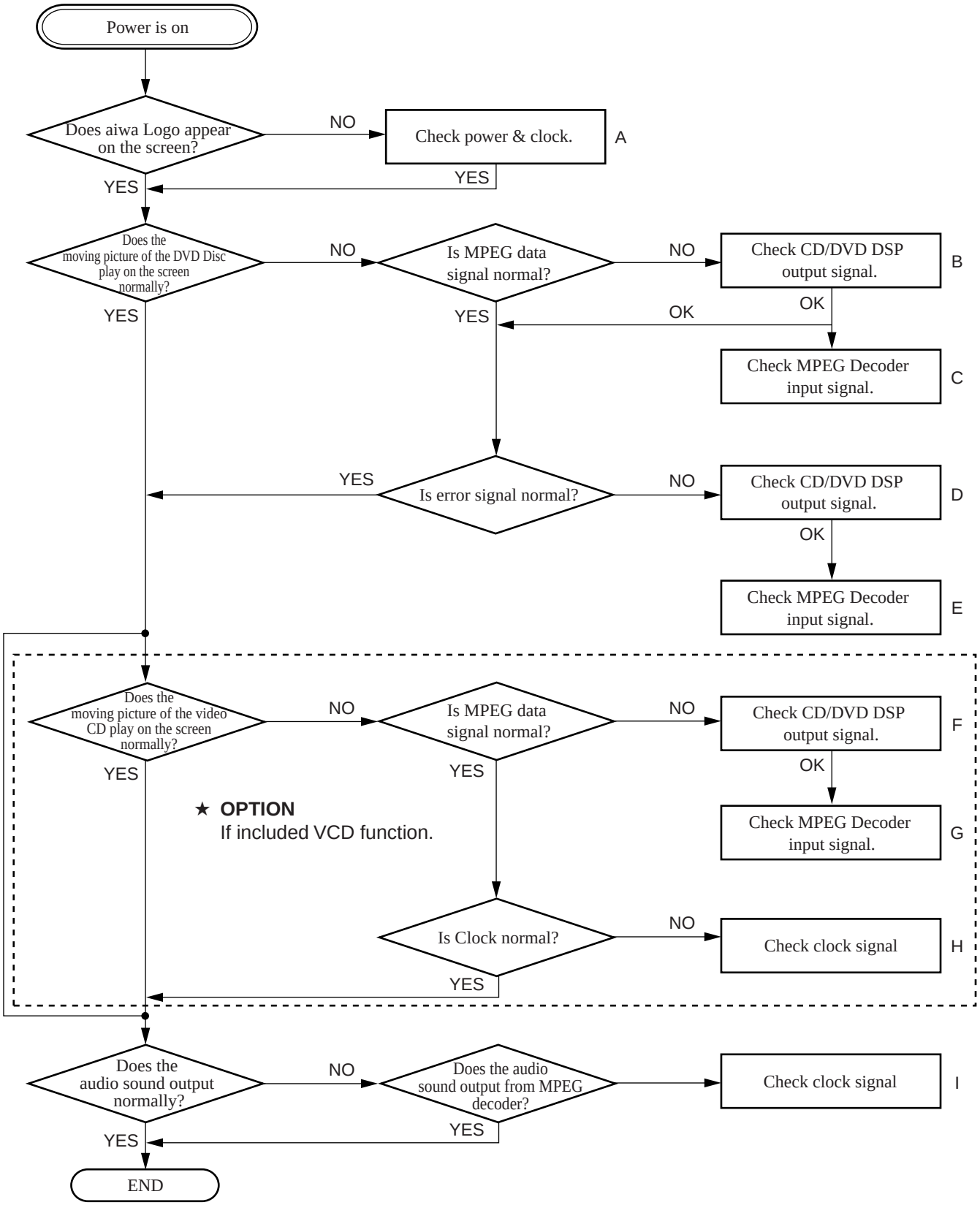
E. Picture abnormal



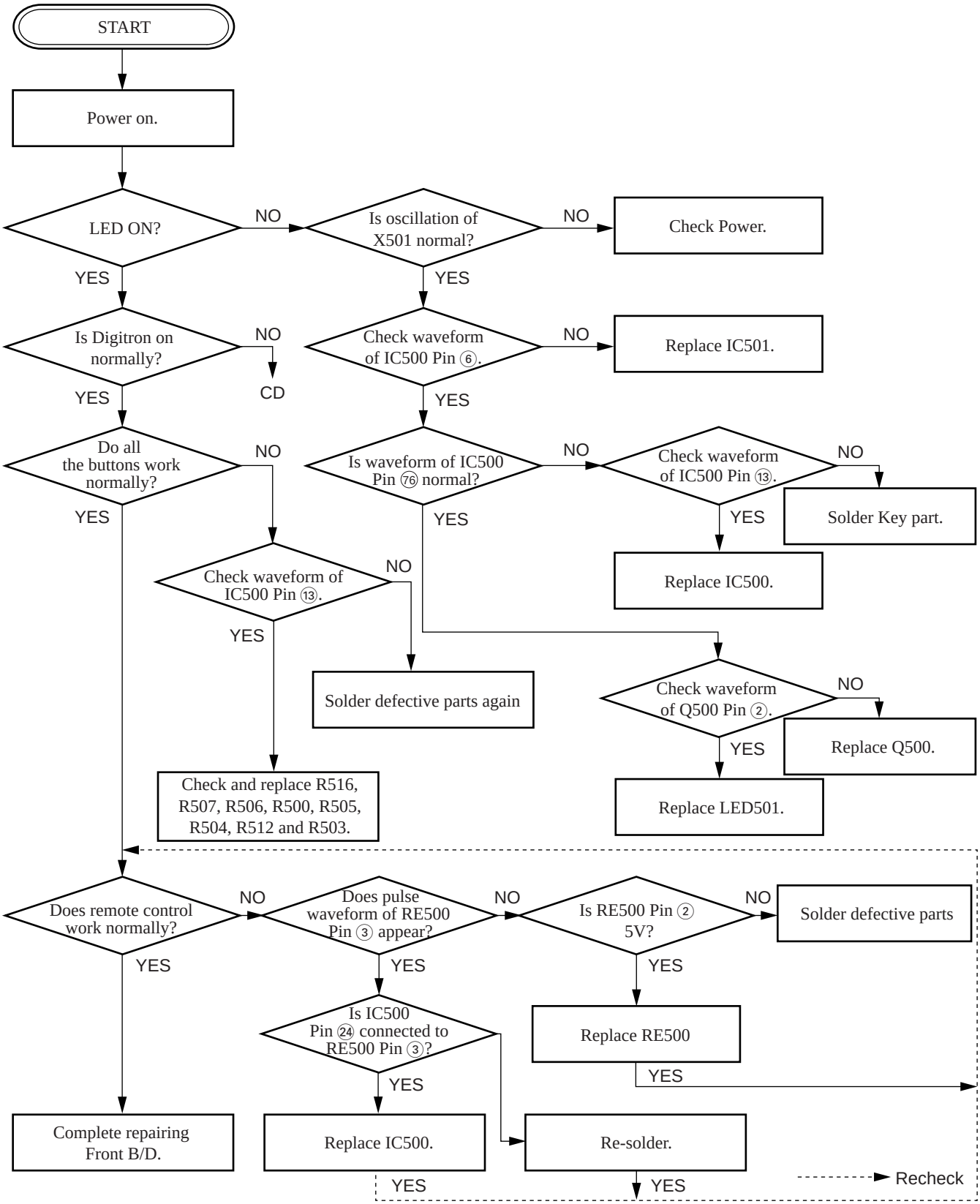
F. Disc Error



3. MPEG Circuit

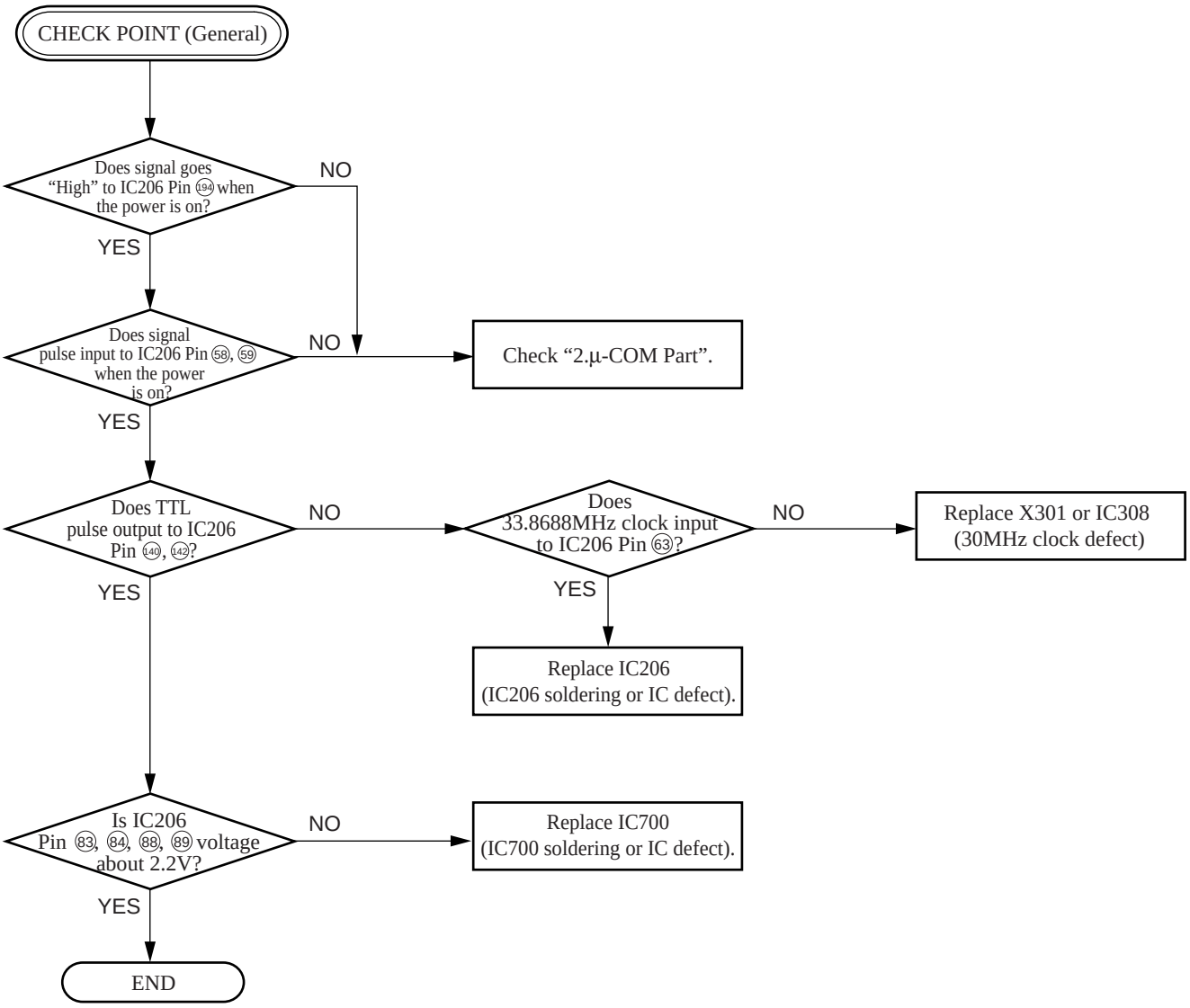


4. Front Circuit (Digitron & key)

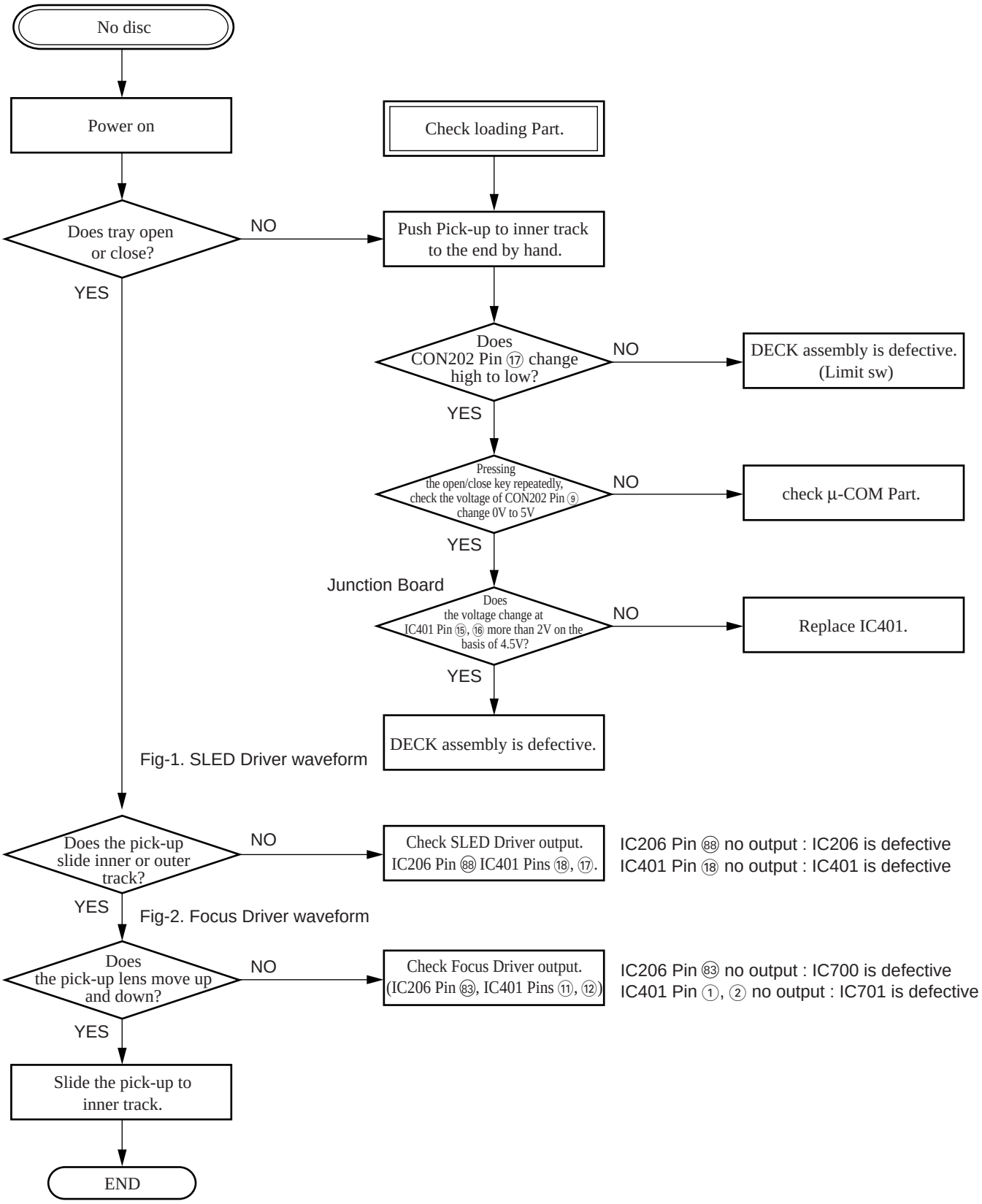


5. RF/Servo Circuit

A.


CHECK POINT (General)
Does signal goes "High" to IC206 Pin ⑭④ when the power is on?
NO
YES
Does signal pulse input to IC206 Pin ⑤⑧, ⑤⑨ when the power is on?
NO
Check "2.μ-COM Part".
YES
Does TTL pulse output to IC206 Pin ①④⓪, ①④②?
NO
Does 33.8688MHz clock input to IC206 Pin ⑥③?
NO
Replace X301 or IC308 (30MHz clock defect)
YES
Replace IC206 (IC206 soldering or IC defect).
YES
Is IC206 Pin ⑧③, ⑧④, ⑧⑧, ⑧⑨ voltage about 2.2V?
NO
Replace IC700 (IC700 soldering or IC defect).
YES
END

B.


No disc
Power on
Does tray open or close?
NO
YES
Check loading Part.
Push Pick-up to inner track to the end by hand.
Does CON202 Pin ⑰ change high to low?
NO
DECK assembly is defective. (Limit sw)
YES
Pressing the open/close key repeatedly, check the voltage of CON202 Pin ⑨ change 0V to 5V
NO
check μ-COM Part.
YES
Junction Board
Does the voltage change at IC401 Pin ⑮, ⑯ more than 2V on the basis of 4.5V?
NO
Replace IC401.
YES
DECK assembly is defective.
Fig-1. SLED Driver waveform
Does the pick-up slide inner or outer track?
NO
Check SLED Driver output. IC206 Pin ⑱ IC401 Pins ⑱, ⑰.
IC206 Pin ⑱ no output : IC206 is defective
IC401 Pin ⑱ no output : IC401 is defective
YES
Fig-2. Focus Driver waveform
Does the pick-up lens move up and down?
NO
Check Focus Driver output. (IC206 Pin ⑧③, IC401 Pins ⑪, ⑫)
IC206 Pin ⑧③ no output : IC700 is defective
IC401 Pin ①, ② no output : IC701 is defective
YES
Slide the pick-up to inner track.
END

C.

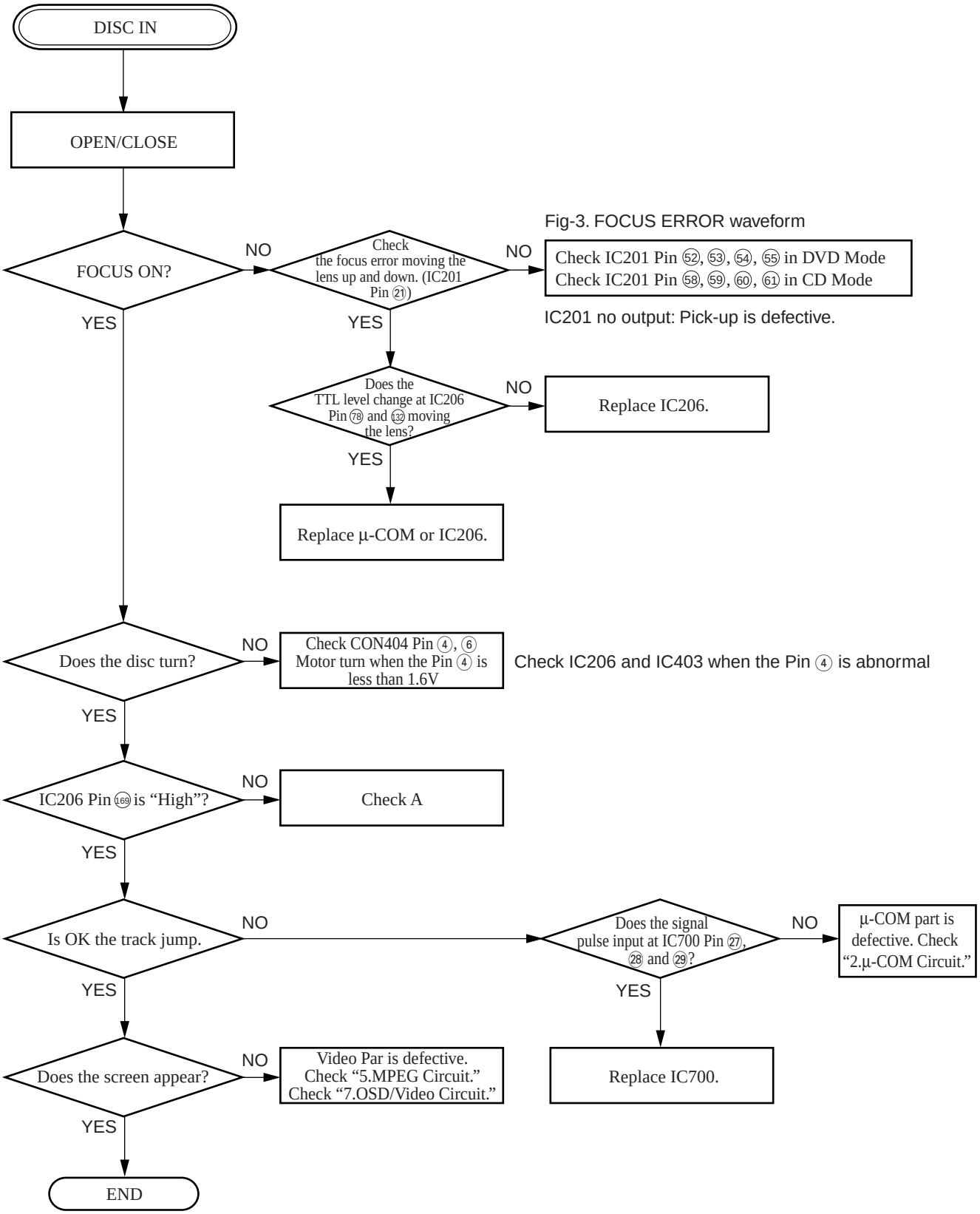
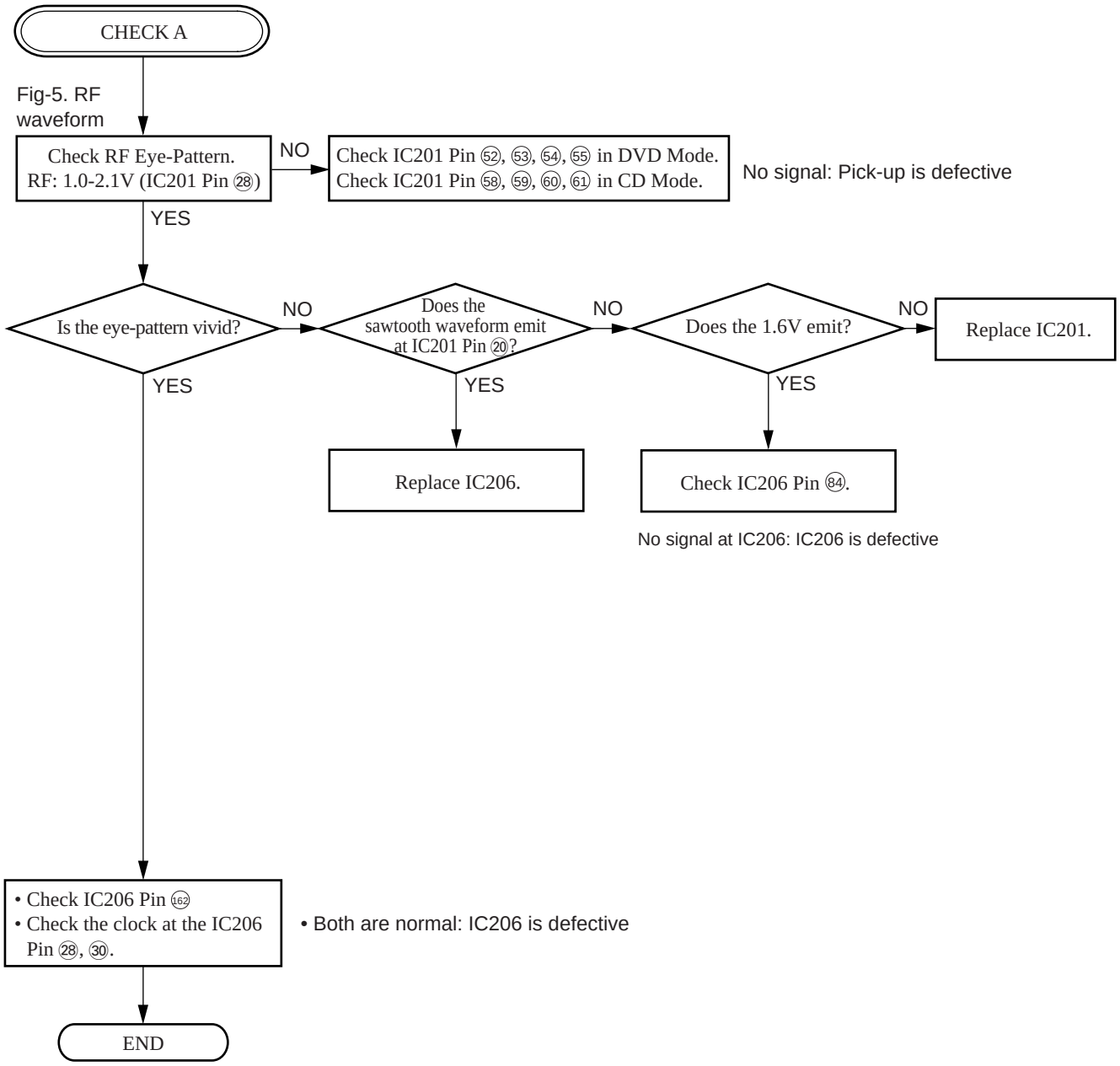
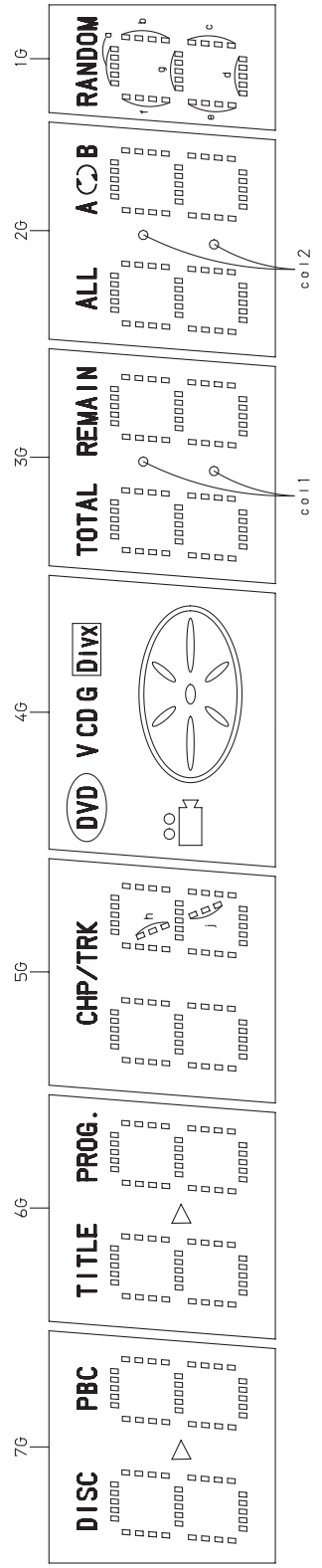


Fig-3. FOCUS ERROR waveform

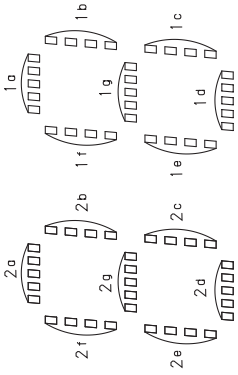
D.


CHECK A
Fig-5. RF waveform
Check RF Eye-Pattern.
RF: 1.0-2.1V (IC201 Pin 28)
NO
Check IC201 Pin 52, 53, 54, 55 in DVD Mode.
Check IC201 Pin 58, 59, 60, 61 in CD Mode.
No signal: Pick-up is defective
YES
Is the eye-pattern vivid?
NO
Does the sawtooth waveform emit at IC201 Pin 20?
NO
Does the 1.6V emit?
NO
Replace IC201.
YES
YES
YES
Replace IC206.
Check IC206 Pin 84.
No signal at IC206: IC206 is defective
• Check IC206 Pin 162
• Check the clock at the IC206 Pin 28, 30.
• Both are normal: IC206 is defective
END

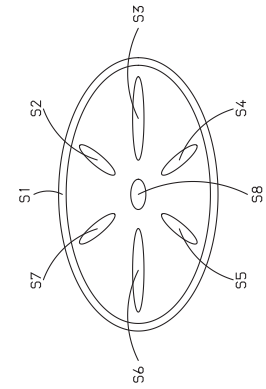
LCD DISPLAY



[7G~5G, 3G, 2G]



[4G]



7-BT-2590K
GRID ASSIGNMENT

	7G	6G	5G	4G	3G	2G	1G
P1	1a	1a	1a	–	1a	1a	a
P2	1b	1b	1b	DVD	1b	1b	b
P3	1f	1f	1f	V	1f	1f	f
P4	1g	1g	1g	CD	1g	1g	g
P5	1c	1c	1c	G	1c	1c	c
P6	1e	1e	1e	DIVX	1e	1e	e
P7	1d	1d	1d	S1	1d	1d	d
P8	▷	▷	–	DivX	col1	col2	–
P9	2a	2a	2a	S2	2a	2a	–
P10	2b	2b	2b	S3	2b	2b	–
P11	2f	2f	2f	S4	2f	2f	–
P12	2g	2g	2g	S5	2g	2g	–
P13	2c	2c	2c	S6	2c	2c	–
P14	2e	2e	2e	S7	2e	2e	–
P15	2d	2d	2d	S8	2d	2d	–
P16	DISC	TITLE	CHP/TRK	–	TOTAL	ALL	RANDOM
P17	PBC	PROG.	–	–	REMAIN	A	–
P18	–	–	1h	–	–	CD	–
P19	–	–	1j	–	–	B	–

Pin No.	Pin Name	I/O	Description
1-6	VID2-7	I	Secondary video input port. Pixel data (TTL compatible) in 8-bit YCrCb format. A higher index corresponds to a greater bit significance. Data on the VID port is latched by rising edge of VIDCLK. (Connected to GND.)
7	VDD	—	Digital power.
8	GND	—	Digital ground.
9	VIDCLK	I	2x pixel clock for secondary video input port. Synchronization circuitry exists for this port to lock it to the primary video port. (Connected to GND.)
10	VIDVALID	I	Video data valid qualifier. A logical 1 indicates data on VID [7:0] is valid data. The sense of this signal is controlled by the VIDVALIDI bit of register 0x1C. (Connected to GND.)
11	VIDVACT	I	Vertical active display region. The sense of this signal is controlled by the VIDVACTI bit of register 0x1C. (Connected to GND.)
12	VIDHACT	I	Horizontal active pixel signal. A logical 1 indicates data on VID [7:0] is in the horizontal display region. The sense of this signal is controlled by the VIDHACTI bit of register 0x1C. (Connected to GND.)
13-16	P0-P3	I	Primary video input port. TTL compatible pixel data in 8-bit YCrCb format. A higher index corresponds to a greater bit significance. (1) Data is latched on the rising edge of the system clock.
17	GND	—	Digital ground. Refer to the PC Board Considerations section of this
18	VDDMAX	—	This pin must be tied to the maximum digital input value. Use 3.3 V if only “3.3 V inputs are used, and 5 V if 5 V inputs are used.”
19-22	P4-P7	I	Primary video input port. TTL compatible pixel data in 8-bit YCrCb format. A higher index corresponds to a greater bit significance. (1) Data is latched on the rising edge of the system clock.
23	BLANK	I	Composite blanking control input (TTL compatible). BLANK is registered on the rising edge of the system clock. The P [7:0] inputs are ignored while BLANK is a logical 0. The sense of this signal is controlled by the BLANKI bit of register 0x19.
24	VSYNC	I/O	Vertical sync input/output (TTL compatible). As an output (master mode “operation), VSYNC is output following the rising edge of the system” “clock. As an input (slave mode operation), VSYNC is registered on the” rising edge of the system clock. The sense of this signal is controlled by the VSYNCI bit of register 0x19.
25	HSYNC	I/O	Horizontal sync input/output (TTL compatible). As an output (master mode “operation), HSYNC is output following the rising edge of the system” “clock. As an input (slave mode operation), HSYNC is registered on the” rising edge of the system clock. The sense of this signal is controlled by the HSYNCI bit of register 0x19.
26	FIELD	O	Field control output (TTL compatible). FIELD transitions after the rising “edge of the system clock, two clock cycles following falling HSYNC. The” sense of this signal is controlled by the FIELDI bit of register 0x19. The state of this pin at power-up determines the default state of the PCLK_SEL “register. If not loaded, this pin will be pulled low with an internal pull-down” resistor.
27	GND	—	Digital ground.
28	VDD	—	Digital power.

Pin No.	Pin Name	I/O	Description
29, 30	ALPHA0, 1	I	“Alpha blend pins. Provides for 1-, 2-, or 4-bit external blend selection” between video and graphic overlay data. Signals are latched using the system clock. (Connected to GND.)
31-36	OSD0-5	I	Dedicated graphic overlay port. Pixel data (TTL compatible) in 8-bit YCrCb format. Signals are latched using the system clock. (Connected to GND.)
37	GND	—	Digital ground.
38	VDD	—	Digital power.
39, 40	OSD6 ,7	I	Dedicated graphic overlay port. Pixel data (TTL compatible) in 8-bit YCrCb format. Signals are latched using the system clock. (Connected to GND.)
41	AGND	—	Analog ground.
42	DACF	O	Component chrominance U channel, component blue, or composite video.
43	DACE	O	Component chrominance V channel, component green, or composite video.
44	DACD	O	“Component luminance, component red, or optional luma-delayed” composite video.
45	VBIAS2		AGND; the capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
46	VAA		Analog power.
47	COMP2		This pin to VAA. The capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. COMP1 is used with DACs A/B/C and COMP2 is used with DACs D/E/F.
48	FSADJ2	I	Full-scale adjust control pin. Resistors RSET1 and RSET2 connected between these pins and AGND controls the full-scale output current on the “analog outputs. For standard operation, use the nominal values shown” under Recommended Operating Conditions. FSADJ2 controls DACs D/E/F.
49	VREF	O	Voltage reference pin.
50	N/C	—	Not used.
51	AGND	—	Analog ground.
52	VAA	—	Analog power.
53	FSADJ1	I	Full-scale adjust control pin. Resistors RSET1 and RSET2 connected between these pins and AGND controls the full-scale output current on the “analog outputs. For standard operation, use the nominal values shown” under Recommended Operating Conditions. FSADJ1 controls DACs A/B/C.
54	COMP1	O	Compensation pin.
55	VAA	—	Analog power.
56	VBIAS1	—	DAC bias voltage.
57	DACC	O	Composite video.
58	DACB	O	Modulated chrominance video signal or optional luma-delayed composite video.
59	DACA	O	Luminance video or optional composite video.
60	AGND	—	Analog ground.
61	GND	—	Digital ground.
62	ALTADDR	I	Alternate slave address input (TTL compatible). A logical 1 corresponds to “write address of 0x88 and a read address of 0x89, while a logical 0” corresponds to a write address of 0x8A and a read address of 0x8B. See the Serial Programming Interface section for more detail. (Connected to GND.)

Pin No.	Pin Name	I/O	Description
63	RESET	I	Reset control input (TTL compatible). Setting to zero resets both video “timing (horizontal, vertical, subcarrier counters to the start of VSYNC of” “first field) and the serial control interface, and resets the registers. RESET” must be a logical 1 for normal operation.
64	VDD	—	Digital power. Refer to the PC Board Considerations section of this
65	GND	—	Digital ground.
66	PGND	—	Dedicated ground for PLL.
67	XTI	I	Crystal input for genlock PLL. (Not used.)
68	XTO	O	Crystal output for genlock PLL. (Not used.)
69	VPLL	—	Dedicated power supply for PLL. (Connected to VDD.)
70	CLKO	O	2x pixel clock for the primary video port. Generated by PLL or pass-through from CLKIN pin. (Not used.)
71	CLKIN	I	2x pixel clock input (TTL compatible).
72	VIDFIELD	I	Field indicator for video input port. A logical 1 indicates data is from an odd field. The sense of this signal is controlled by the VIDFIELDI bit of register 0x1C. (Connected to GND.)
73	TTXREQ	O	Teletext request output (TTL compatible). (Connected to VDD.)
74	TTXDAT	I	Teletext bit stream input (TTL compatible). (Connected to GND.)
75	SID	I/O	Serial interface data input/output (TTL compatible). Data is written to and read from the device via this serial bus.
76	SIC	I	Serial interface clock input (TTL compatible). The maximum clock rate is 400 kHz.
77	GND	—	Digital ground.
78	VDD	—	Digital power.
79, 80	VID0, 1	I	Secondary video input port. Pixel data (TTL compatible) in 8-bit YCrCb format. A higher index corresponds to a greater bit significance. Data on the VID port is latched by rising edge of VIDCLK. (Connected to GND.)

Pin No.	Pin Name	I/O	Description
1	P100	I/O	Programmable I/O pins.
2-4	HDATA0-2	I/O	8-bit bi-directional host data bus. Host writes data to the decoder Code FIFO via HDATA [7:0]. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HDATA [7:0].
5	VDD_3.3	—	3.3-V supply voltage for I/O signals.
6	HDATA3	I/O	8-bit bi-directional host data bus. Host writes data to the decoder Code FIFO via HDATA [7:0]. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM/ROM via HDATA [7:0].
7	VSS	—	Ground for core logic and I/O signals.
8-11	HDATA4-7	I/O	8-bit bi-directional host data bus. Host writes data to the decoder Code FIFO via HDATA [7:0]. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal egisters and local SDRAM/ROM via HDATA [7:0].
12	VDD_2.5	—	2.5-V supply voltage for core logic.
13	RESET	I	Hardware reset. An external device asserts RESET (activeLOW) to execute a decoder hardware reset. “ To ensure proper initialization after power is stable, assert RESET for at least 20 ms.”
14	VSS	—	Ground for core logic and I/O signals.
15	/WAIT	O	Transfer not complete/data acknowledge. Active LOW to indicate host initiated transfer is not complete. WAIT is asserted after the falling edge of CS and reassertedwhendecoderis ready to “complete transfer cycle. Open drain signal,” must be pulled-up via 1kW to 3.3 volts. Driven high for 10 ns before tristate.
16	/INT	O	“Host interrupt. Open drain signal, must be pulled-up via 4.7kW to 3.3 volts. Driven high for” 10 ns before tristate.
17	VDD	—	3.3-V supply voltage for I/O signals.
18	/AMWE	—	Not used.
19	VSS	—	Ground for core logic and I/O signals.
20			
21-26	HDATA8-13	I/O	Programmable I/O pins. Input mode after reset.
27	VDD	—	3.3-V supply voltage for I/O signals.
28	HDATA14	I/O	Programmable I/O pins. Input mode after reset.
29	VSS	—	Ground for core logic and I/O signals.
30	HDATA15	I/O	Programmable I/O pins. Input mode after reset.
31-35	HADDR12-16	I/O	Programmable I/O pins. Output mode after reset.
36	VDD	—	3.3-V supply voltage for I/O signals.
37	HADDR17	I/O	Programmable I/O pins. Output mode after reset.
38	VSS	—	Ground for core logic and I/O signals.
39	HADDR18	I/O	Programmable I/O pins. Output mode after reset.
40	VDD	—	2.5-V supply voltage for core logic.
41	HADDR19	I/O	Programmable I/O pins. Output mode after reset.
42	VSS	—	Ground for core logic and I/O signals.
43-46	HADDR20-23	I/O	Programmable I/O pins. Output mode after reset.

Pin No.	Pin Name	I/O	Description
47	VDD	—	3.3-V supply voltage for I/O signals.
48	BEO	I/O	Programmable I/O pins. Output mode after reset.
49	VSS	—	Ground for core logic and I/O signals.
50, 51	NC	O	No Connection
52	P101	I/O	Programmable I/O pins.
53, 54	MDATA15, 0	I/O	Memory data.
55	VDD	—	3.3-V supply voltage for I/O signals.
56	MDATA14	I/O	Memory data.
57	VSS	—	Ground for core logic and I/O signals.
58-60	MDATA1, 13, 2	I/O	Memory data.
61	VDD_3.3	—	3.3-V supply voltage for I/O signals.
62	MDATA12	I/O	Memory data.
63	VSS	—	Ground for core logic and I/O signals.
64	MDATA3	I/O	Memory data.
65	VDD	—	2.5-V supply voltage for core logic.
66	MDATA11	I/O	Memory data.
67	VSS	—	Ground for core logic and I/O signals.
68	MDATA4	I/O	Memory data.
69	VDD	—	3.3-V supply voltage for I/O signals.
70	MDATA10	I/O	Memory data.
71	VSS	—	Ground for core logic and I/O signals.
72-74	MDATA5, 9, 6	I/O	Memory data.
75	VDD	—	3.3-V supply voltage for I/O signals.
76	MDATA8	I/O	Memory data.
77	VSS	—	Ground for core logic and I/O signals.
78	MDATA7	I/O	Memory data.
79	LDQM	O	SDRAM LDQM.
80	UDQM	O	SDRAM UDQM.
81	VDD	—	3.3-V supply voltage for I/O signals.
82	/MWE	O	SDRAM write enable. Decoder asserts active LOW to request a write operation to the SDRAM array.
83	VSS	—	Ground for core logic and I/O signals.
84	SD-CLK	O	SDRAM system clock.
85	/SD-CAS	O	Active LOW SDRAM column address.
86	/SD-RAS	O	Active LOW SDRAM row address.
87	VDD	—	3.3-V supply voltage for I/O signals.
88	SD-CS1	O	Active LOW SDRAM bank select.
89	VSS	—	Ground for core logic and I/O signals.
90	SD-CS0	O	Active LOW SDRAM bank select.
91	VDD	—	2.5-V supply voltage for core logic.
92	NC	O	No Connection.

Pin No.	Pin Name	I/O	Description
93	VSS	—	Ground for core logic and I/O signals.
94	NC	O	No Connection
95	VDD	—	3.3-V supply voltage for I/O signals.
96	MADDR9	O	Memory address.
97	VSS	—	Ground for core logic and I/O signals.
98-100	MADDR1, 8, 10	O	Memory address.
101	VDD	—	3.3-V supply voltage for I/O signals.
102	MADDR7	O	Memory address.
103	VSS	—	Ground for core logic and I/O signals.
104-106	MADDR0, 8, 1	O	Memory address.
107	VDD	—	3.3-V supply voltage for I/O signals.
108	MADDR5	O	Memory address.
109	VSS	—	Ground for core logic and I/O signals.
110-112	MADDR2, 4, 3	O	Memory address.
113	VDD	—	3.3-V supply voltage for I/O signals.
114	MADDR12	O	Memory address.
115	VSS	—	Ground for core logic and I/O signals.
116	MADDR13	O	Memory address.
117	VDD	—	2.5-V supply voltage for core logic.
118	MADDR14	O	Memory address.
119	VSS	—	Ground for core logic and I/O signals.
120-122	MADDR15-17	O	Memory address.
123	VDD	—	3.3-V supply voltage for I/O signals.
124	MADDR18	O	Memory address. (Not used.)
125	VSS	—	Ground for core logic and I/O signals.
126, 127	MADDR19, 20	O	Memory address. (Not used.)
128	/ROM_CS	O	Open drain signal, must be pulled-up via 4.7kW to 3.3 volts.
129	P102	I/O	Programmable I/O pins.
130	NC	O	No Connection.
131, 132	VDD	—	3.3-V supply voltage for I/O signals.
133	P103	I/O	Programmable I/O pins.
134, 135	VDD	—	3.3-V supply voltage for I/O signals.
136	VSS	—	Ground for core logic and I/O signals.
137	VDD	—	3.3-V supply voltage for I/O signals.
138	P104	I/O	Programmable I/O pins.
139, 140	VDD	—	3.3-V supply voltage for I/O signals.
141	P105	I/O	Programmable I/O pins.
142, 143	VDATA0, 1	O	Video data bus. Byte serial CbYCrY data synch- ronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoderuses configuration parameters to drive or 3-state VDATA.
144	VDD	—	2.5-V supply voltage for core logic.

Pin No.	Pin Name	I/O	Description
145	VDATA2	O	Video data bus. Byte serial CbYCrY data synch- ronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoderuses configuration parameters to drive or 3-state VDATA.
146	VSS	—	Ground for core logic and I/O signals.
147	P105	I/O	Programmable I/O pins.
148	VDATA3	O	Video data bus. Byte serial CbYCrY data synch- ronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoderuses configuration parameters to drive or 3-state VDATA.
149	VDD	—	3.3-V supply voltage for I/O signals.
150	VDATA4	O	Video data bus. Byte serial CbYCrY data synch- ronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoderuses configuration parameters to drive or 3-state VDATA.
151	VSS	—	Ground for core logic and I/O signals.
152	VDATA5	O	Video data bus. Byte serial CbYCrY data synch- ronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoderuses configuration parameters to drive or 3-state VDATA.
153	P107	I/O	Programmable I/O pins.
154, 155	VDATA6, 7	O	Video data bus. Byte serial CbYCrY data synch- ronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoderuses configuration parameters to drive or 3-state VDATA.
156	P108	I/O	Programmable I/O pins.
157	/HSYNC	I/O	Horizontal sync. The decoder begins out putting pixel data for a new horizontal line after the falling (active) edge of HSYNC.
158	/VSYNC	I/O	Vertical sync. Bi-directional, the decoder outputs the top border of a new field on the first HSYNC after the falling edge of VSYNC. VSYNC can accept vertical synchronization or top/bottom field notification from an external source. (VSYNC HIGH = bottom fie
159	DA-IEC	O	Bitstream data in IEC-1937 or PCM data out in IEC-958 format.
160	VDD	—	3.3-V supply voltage for I/O signals.
161	DA-DATA0	O	PCM data out, eight channels. Serial audio samples relative to DA-BCK clock.
162	VSS	—	Ground for core logic and I/O signals.
163-165	DA-DATA1-3	O	PCM data out, eight channels. Serial audio samples relative to DA-BCK clock.
166	DA-LRCK	O	PCM left-right clock. Identifies the channel for each audio sample. the polarity is programmable.
167	DA-BCK	O	PCM bit clock. Divided by 8 from DA-XCK, DA-BCK can be either 48 or 32 times the sampling clock.
168	VDD	—	2.5-V supply voltage for core logic.
169	DA-XCK	I/O	Audio master frequency clock. Used to generate DA-BCK and DA-LRCK. DA-XCK can be either 384 or 256 times the sampling frequency.
170	VSS	—	Ground for core logic and I/O signals.
171	DAI-DATA	I	PCM input data, two channels. Serial audio samples relative to DAI-BCK clock.
172	DAI-LRCK	I	PCM input left-right clock.

Pin No.	Pin Name	I/O	Description
173	DAI-BCK	I	PCM input bit clock.
174	P109	I/O	Programmable I/O pins.
175	CLKSEL	I	Clock Select: Internal = VDD, External = VSS
176	A_VDD	—	3.3-V analog supply voltage.
177	VCLK	I	Video clock. Clocks out data on input. VDATA [7:0]. Clock is typically 27 MHz.
178	SYSCLK	I	System clock. Decoderrequires an external 27MHz TTL oscillator. Drive with the same 27-MHz as VCK.
179	A-VSS	—	Analog ground for PLL.
180	DVD-DATA0/CD-DATA	I	Serial CD data. This pin is shared with DVD compressed data DVD-DATA0. ERROR 200 I Error in input data. If ERROR signal is not available from the DSP it must be grounded.
181	VDD	—	3.3-V supply voltage for I/O signals.
182	DVD-DATA1/CD-LRCK	I	Programmable polarity 16-bit word synchronization to the decoder (right channel HIGH). This pin is shared with DVD compressed data DVD-DATA1.
183	VSS	—	Ground for core logic and I/O signals.
184	DVD-DATA2/CD-BCK	I	CD bit clock. Decoder acceptmultipleBCKrates. This pin is shared with DVD compressed data DVD-DATA2.
185	DVD-DATA3/CD-C2PO	I	Asserted HIGH indicates a corrupted byte. Decoder keeps the previous valid picture on-screen until the next valid picture is decoded. This pin is shared with DVD compressed data DVD-DATA3.
186-189	DVD-DATA4/ CDG_SDATA	I	DVD parallel compressed data from DVD DSP. When DVD DSP sends 32-bit words, it must write the DVD-DATA5/CDG_VFSY MSB first. CDG-SDATA: CD+G (Subcode) Data. DVD-DATA6/CDG_SOSI Indicates serial subcode data input. DVD-DATA7/CDG_SCLK CDG-VSFY: CD+G (Subcode) Frame Sync. Indicates frame-start or composite synchronization input. CDG-S0S1: CD+G (Subcode) Block Sync. Indicates block-start synchronization input. CDG-SCLK: CD+G (Subcode) Clock. Indicates subcode data clock input or out-put.
190	PI101	I/O	Programmable I/O pins.
191	VREQUEST	O	Video request. Decoder asserts VREQUEST to indicate that the video input buffer has available space. Polarity is programmable.
192	VSTROBE	I	Video strobe. Programmable dual mode pulse. Asynchronous and synchronous. In Asynchronous mode, anexternal sourcepulses VSTROBE to indicate data is ready for transfer. In synchronous mode VSTROBE clocks data.
193	VDD	—	3.3-V supply voltage for I/O signals.
194	AREQUEST	O	Audio request. Decoder asserts AREQUEST to indicate that the audio input buffer has available space. (Not used.)
195	VSS	—	Ground for core logic and I/O signals.
196	V-DACK/ASTROBE	I	In synchronous mode, Video data acknowledge. Asserted when DVD data is valid. Polarity is programmable. In asynchronous mode, data strobing for audio bit stream input.
197	VDD	—	2.5-V supply voltage for core logic.

Pin No.	Pin Name	I/O	Description
198	A-DACK	I	Audio data acknowledge.
199	VSS	—	Ground for core logic and I/O signals.
200			
201	HOST&SEL	I	Pull up.
202-204	HADDR0-2	I	Host address bus. 3-bit address bus selects one of eight host interface registers.
205	DTACKSEL	I	Tie HIGH to select WAIT signal, LOW to select DTACK signal (Motorola 68K mode).
206	/CS	I	Host chip select. Host asserts CS to select the decoder for a read or write operation. The falling edge of this signal triggers the read or write operation.
207	R/W	I	Read/write strobe in M mode. write strobe in I mode. Host asserts R/W LOW to select write and
208	/RD	I	Read strobe in I mode. Must be held HIGH in M Mode LOW to select Read.

IC, GDC25D801

Pin No.	Pin Name	I/O	Description
1-16	DAT1-16	I/O	Bi-directional data to DRAM.
17	VSS	—	Digital GND.
18-21	ADD1-4	O	Address output to DRAM.
22	VDD	I	Digital power supply.
23-27	ADD5-9	O	Address output to DRAM.
28	X2_MCK	I	Master clock from oscillator for 2x decoding.
29	VSS	—	Digital GND.
30	MCK	I	Master clock from oscillator.
31	VDD	—	Digital power supply.
32	RAS	O	Row address strobe to DRAM.
33	UCAS	O	Column address upper byte control strobe to DRAM.
34	LCAS	O	Column address lower byte control strobe to DRAM.
35	WE	O	Write enable signal to DRAM.
36	OE	O	Output enable signal to DRAM.
37	SCAN_IN	I	Scan data input (Not used.)
38	TEST_SE	I	Test mode selection (low for normal) (Connected to GND.)
39-45	TEST_OUT12-6	O	Test output (Not used.)
46	T_SEL	I	Test selection : 0 for normal.
47-52	TEST_OUT5-0	O	Test output (Not used.)
53-56	TEST_SEL0-3	I	Test mode output selection.
57	TESTSERVO	I	TEST PIN (NORMAL STATE = H) (Connected to VDD.)
58	E_SIN	I	SERVO DSP PGM. DOWNLOADING DATA INPUT.
59	E_CLK	I	SERVO DSP PGM. DOWNLOADING CLK.
60	E_ENB	I	SERVO DSP DOWNLOADING ENABLE.
61	E_DRB	I	SERVO DSP PGM. DOWNLOADING DIRECTION.
62	VSS	—	Digital GND.
63	SERVO CLK	I	SERVO DSP CLOCK INPUT.
64	E_SOUT	O	SERVO DSP PGM. DOWNLOADING DATA OUTPUT.
65	VDD	—	Digital power supply.
66-68	E_ST0-2	O	SERVO DSP DOWNLOADING STATUS 0-2.
69	GPIO7	I/O	SERVO DSP GENERAL I/O: FSON (FOCUS OK INVERTING).
70	GPIO6	I/O	SERVO DSP GENERAL I/O: PSEL.
71	GPIO5	I/O	SERVO DSP GENERAL I/O: ADADDR3 (Not used.)
72	GPIO4	I/O	SERVO DSP GENERAL I/O: FKRST (Not used.)
73	GPIO3	I/O	SERVO DSP GENERAL I/O: FKSET (Not used.)
74	GPIO2	I/O	SERVO DSP GENERAL I/O: FEL (Not used.)
75	GPIO1	I/O	SERVO DSP GENERAL I/O.
76	GPIO0	I/O	SERVO DSP GENERAL I/O: DSP_SENSE.
77	VSS	—	Digital GND.
78	SENS	O	SERVO DSP INTERNAL STATUS MONITOR.
79	VDD	—	Digital power supply.

Pin No.	Pin Name	I/O	Description
80	SCLK	I	Serial Command CLOCK.
81	SDATA	I	Serial Command DATA.
82	XLAT	I	Serial Command LATCH.
83	AOUT1	O	TDF.
84	AOUT2	O	TDF.
85	AVDD	—	Analog power supply for ADC.
86	VCM	I	TDF.
87	AGND	—	Analog GND for ADC.
88	AOUT3	O	TDF.
89	AOUT4	O	TDF.
90	DGND	—	Digital GND for ADC.
91	RFVCM	I	TDF (Connected to VREF.)
92	DVDD	—	Digital power supply for ADC.
93	AGND	—	Analog GND for ADC.
94	VREFN	I	TDF.
95	VREFP	I	TDF.
96	INP	I	TDF (Connected to VREF.)
97	AGND	—	Analog GND for ADC.
98	AIN4	I	TDF (Connected to VREF.)
99	AIN3	I	TDF.
100	AVDD	—	Analog power supply for ADC.
101	AIN2	I	TDF.
102	AIN1	I	TDF.
103	AIN0	I	TDF.
104	ADCVCM	I	TDF (Connected to VREF.)
105	SCK	O	PLL clock output.
106-111	EXT_AD0-5	I	ADC data input (Not used.)
112	SELEFM	I	EFMDATA INPUT SELECTION (Connected to GND.)
113	EXCK	I	SUB DATA REQUEST INPUT (Not used.)
114	SQCK	I	SUB Q DATA REQUEST.
115	C16M	O	5.6448 MHz (DIGITAL OUT CLOCK) (Not used.)
116	DOTX	O	CD DIGITAL DATA OUTPUT (Not used.)
117	VDD	—	Digital power supply.
118	SQSO	O	SUB Q DATA OUTPUT.
119	VSS	—	Digital GND.
120	PWMCH1	O	PWM CHANNEL1 (x3 CARRIER).
121	PWMCH2	O	PWM CHANNEL1 (x3 CARRIER).
122	PWMCH3	O	PWM CHANNEL1 (x3 CARRIER): SLED DRIVE OUTPUT.
123	PWMCH4	O	PWM CHANNEL1 (x1 CARRIER): PDO_CTR PWM OUTPUT.
124	PWMCH5	O	PWM CHANNEL1 (x1 CARRIER): RF_GAIN_CTL PWM OUTPUT.
125	PWMCH6	O	PWM CHANNEL1 (x1 CARRIER): TE_BAL_CTL PWM OUTPUT.

Pin No.	Pin Name	I/O	Description
126	DEFECT_IN_A	I	EXTERNAL DEFECT INPUT PIN.
127	SI_ENC1	I	SLED ENCODER1 INPUT.
128	SI_ENC2	I	SLED ENCODER2 INPUT (Connected to GND.)
129	TZC	I	TRACK CROSS PULSE 2 INPUT.
130	MIRR	I	TRACK CROSS PULSE 1 INPUT.
131	MSDATAO	O	SERVO DSP INTENAL STATUS SERIAL OUTPUT.
132	FOK	O	INTERNAL GENERATED FOK (Focus OK) H=OK.
133	VDD	—	Digital power supply.
134	DEFECT	O	INTERNAL GENERATED DEFECT: H=DEFECT.
135	VSS	—	Digital GND.
136	SLD_FG	O	SLD_FG=(SL_ENC1) XOR (SL_ENC2) (Not used.)
137	C_SIG	O	TRACK CROSS PULSE.
138	COMP	O	TRACK CROSS MONITOR (Not used.)
139	INT1_	O	SERVO DSP INTERRUPT 1 MONITOR (MICOM COMMAND INT) (Not used.)
140	INT2_	O	SERVO DSP INTERRUPT 2 MONITOR (FOCUS SERVO INT) (Not used.)
141	VSS	—	Digital GND.
142	INT3_	O	SERVO DSP INTERRUPT 1 MONITOR (TRACK SERVO INT) (Not used.)
143	INT4_	I	SERVO DSP INTERRUPT 1 MONITOR (Not used.)
144	VDD	—	Digital power supply.
145	PADCSB	I	A/D 7824 OUTPUT ENABLE (LOW ACTIVE) (Not used.)
146	ADCOMP	I	A/D 7824 A/D CONVERTER A/D CONVERSION END STATUS (Not used.)
147-154	VDCDATA0-7	I	A/D 7824 A/D CONVERTER DATA BUS0-7. (Connected to GND.)
155	ADADDR0	O	A/D 7824 A/D CONVERTER ADDRESS (Not used.)
156	DVDD	—	Digital power supply for ADC.
157	ADADDR1	I	A/D 7824 A/D CONVERTER ADDRESS (Not used.)
158	DGND	—	Digital GND for ADC.
159	AGND	—	Analog GND for ADC.
160	VRT	I	TDF.
161	AVDD	—	Analog power supply for ADC.
162	RF	I	TDF.
163	VRM	I	TDF.
164	VRB	I	TDF.
165	MDS	O	Spindle motor control signal (Not used.)
166	MDP	O	Spindle motor control signal (Not used.)
167	OVER64	O	Not used.
168	MON	O	Spindle motor ON/OFF control signal.
169	LOCK	O	CLV servo lock signal.
170	FG_M	I	TDF.
171	VSS	—	Digital GND.
172	SCAN_OUT	O	SCAN DATA OUTPUT (Not used.)
173	VDD	—	Digital power supply.

Pin No.	Pin Name	I/O	Description
174	INT	O	Interrupt request to Host.
175	RN	I	Read strobe from HOST.
176	WN	I	Write strobe from HOST.
177	CS	I	Chip select from HOST.
178-183	A0-5	I	Internal register address from HOST.
184	VSS	—	Digital GND.
185	PS0	I	Bi-directional data to HOST.
186	VDD	—	Digital power supply.
187-193	PS1-7	I/O	Bi-directional data to Host.
194	RESET	I	HARDWARE RESET.
195	REQ_DIVX	I	Data request from DIVX module.
196	REQ_MPEG	I	Data request from MPEG.
197-204	MPEG1-8	O	MPEG data.
205	SENB	O	MPEG data valid signal (low for valid).
206	SDCLK	O	MPEG data transfer clock.
207	SERR	O	MPEG data error detection signal (low indicates error occurred).
208	SYNC	O	MPEG data sector sync. signal.

IC, HD6417034AFI20

Pin No.	Pin Name	I/O	Description
1	Z06	I/O	SUB Q Code Sync Detection Signal (CD Disc Mode).
2	DSP_INT	I/O	1. Interrupt request signal to µ-COM (DVD disc mode). 2. Type: a. Track miss occurred b. Search End c. New sector out start d. DSI data is ready e. New sector in f. System data is ready g. Back track jump request
3	GND	I	GND.
4-11	D00-D07	I/O	Data Line 00-07.
12	GND	I	GND.
13, 14	D08, D09	I/O	Data Line 08, 09.
15	VCC	I	5VD.
16-21	D10-D15	I/O	Data Line 10-15.
22	GND	I	GND.
23-30	A00-A07	O	Address Line 00-07.
31	GND	I	GND.
32-39	A08-A15	O	Address Line 08-15.
40	GND	I	GND.
41, 42	A16, A17	O	Address Line 16, 17.
43	VCC	I	5VD.
44-47	A18-A21	O	Address Line 18-21.
48	/ROM_CS	O	Chip Enable For Flash ROM.
49	/CASH	O	CAS for Higher Byte for DRAM.
50	/IOCS1	O	Chip Enable to Multiplexer (IC101).
51	/CASL	O	CAS for Lower Byte for DRAM.
52	GND	I	GND.
53	BCA_CODE	I/O	BCA Code Input when DIVX Disc Mode → Not used.
54	/RAS	I/O	RAS for DRAM.
55	DPLL_L	I/O	Digital PLL IC Serial Data Latch Out.
56	/MICOM_WAIT	I/O	MPEG IC Internal Status Serial Input.
57	/WR	I/O	Write Signal for DRAM/FlashROM/DSP/MPEG.
58	E_SOUT	I/O	Servo DSP Program Downloading Data Out.
59	/RD	I/O	Read Signal for DRAM/FlashROM/DSP/MPEG.
60	DSP_SENSE	I/O	Command response signal (SERVO/DSP → µ-COM).
61	GND	I	GND.
62	E_SIN	I/O	Servo DSP Program Downloading Data IN.
63	E_CLK	I/O	Servo DSP Program Downloading Clock.
64	MPEG_WR	I/O	MPEG and Host I/F Read/Write Control Output.
65	M_REQ	I/O	Serial Communication Request to Front µ-COM.

Pin No.	Pin Name	I/O	Description
66	F_REQ	I/O	Serial Communication Request from Front µ-COM.
67	/STROBE	I/O	Flash ROM Download I/F (Data Strobe in).
68	SENS_MCOM	I/O	1. Servo Event detection signal input 2. Type: a. Focus Error S-curve detection b. 1 track jump completed c. 10 track jump completed d. etc
69	MPEG_INT	I/O	Interrupt Input from MPEG (IC301).
70	VCC	I	5VD.
71	NC	—	NC.
72	GND	I	GND.
73	X1	I	Crystal (20MHz) Input.
74	X2	O	Crystal (20MHz) Output.
75	VCC	I	5VD.
76	NC	—	
77	VCC	I	
78	NC	—	NC.
79	MICOM_RESET	I	Low Active Reset Input from Front.
80	VCC	I	5VD.
81, 82	GND	I	GND.
83-85	VCC	I	5VD.
86	VCC	I	3.3VD.
87	SBADD	I	SBADD (Sub Beam Add) Signal Input from RF IC → Not used.
88	ECHO	I	DC voltage of Echo Volume Input.
89	MIC_A	I	Mic Audio Signal Input for Karaoke Score Function → Not used.
90	DISC_A	I	Disc Audio Signal Input for Karaoke Score Function → Not used.
91	GND	I	GND.
92	F/R	I	Spindle Rotation direction Input from Spindle Motor IC.
93	LOCK	I	CLV Servo Locking Signal Input from DSP IC.
94	DEFECT	I	DISC DEFECT DETECTION Signal Input (Active High).
95	FOK	I	FOCUS OK signal (H=OK) from DSP.
96	GND	I	GND.
97	IIC_DATA	I/O	IIC Bus Data for EEPROM (IC114) and Video ENCODER.
98	IIC_CLK	I/O	IIC Bus Clock for EEPROM (IC114) and Video ENCODER.
99	VCC	I	5VD.
100	LOAD_FR	I/O	Tray Open and Close Control output.
101	MSDATA0	I/O	Servo DSP IC Internal Status Serial Input.
102	S_DATA	I/O	Serial command interface port between RF or SERVO/DSP IC and µ-COM.
103	S_CLK	I/O	
104	SLD_FG	I/O	Sled Motor FG Input.
105	SPINDLE_FG	I/O	Input the FG Signal of Spindle Motor.

Pin No.	Pin Name	I/O	Description
106	GND	I	GND.
107	RXDO	I/O	Serial Data Input from Front.
108	TXDO	I/O	Serial Data OUT to Front.
109	SQSO	I/O	SUB Q Data Input from Servo & DSP IC.
110	MODE_SW	I/O	Program Download mode detect (Download mode is “L”).
111	SCKO	I/O	Serial Interface Clock to Front.
112	SQCK	I/O	SUB Q Data Request to Servo & DSP IC.

IC, LC866112B-5N21

Pin No.	Pin Name	I/O	Description
1	P35	I	Select down SW input from CN505 (SW509).
2	P36	I	Enter SW input from SW501.
3	P37	I	Select right SW input CN505 (SW509).
4	PWM1	O	Not used.
5	TEST1	—	Not used (Test port).
6	/RES	I	Reset signal input from IC501 3 pin.
7	XT1	I	Not used (Input for 32.768kHz crystal oscillation).
8	XT2	O	Not used (Output for 32.768kHz crystal oscillation).
9	VSS	—	GND.
10	CF1	I	Ceramic resonator X501 (6MHz) oscillation input.
11	CF2	O	Ceramic resonator X501 (6MHz) oscillation output.
12	VDD	—	VCC (5V).
13	P80	I	KEY IN input from CN504.
14, 15	P81, P82	I	Reserved.
16	P83	I	Shuttle 3 line A/D input.
17-20	P84-P87	I	Not used.
21	MODE_SW	I/O	“LOW” at program download mode.
22	M_REQ	I	Request signal (Active “LOW”) from IC108 (Main µ-COM, SH7034).
23	P72	I	Not used.
24	P73	I	Remocon receiver signal input.
25-31	G1-G7	O	VFD display control signal output. DIG 501 G1 to G7.
32-40	P1-P9	O	VFD display control signal output. DIG 501 P1 to P9.
41	VPP	I	VCC (5VAU).
42	VKK	I	-27V from CN503 (SMPS).
43-52	P10-P19	O	VFD display control signal output. DIG 501 P10 to P19.
53-56	S26-S29	—	Not used.
57	S30	—	D503 option (Present at AIWA remocon model).
58	S31	—	Not used.
59	P00	—	Diode option input.
60-64	P01-P05	—	Not used.
65	ZOOM_RST	I/O	
66	V07	—	
67	VSS	—	GND.
68-70	P10-P12	—	Reserved.
71	F_RXD	O	Serial data to IC108 (Main µ-COM, SH7034).
72	F_TXD	I	Serial data input from IC108 (Main µ-COM, SH7034).
73	F_CLK	I	Serial clock input from IC108 (Main µ-COM, SH7034).
74	F_REQ	O	Request signal (Active “LOW”) to IC108 (Main µ-COM, SH7034).
75	M_RESET	O	Reset signal (Active “LOW”) to IC108 (Main µ-COM, SH7034).
76	PWR_CTL	O	Power control (Active “HIGH”) to main board.
77	P31	I/O	Not used.

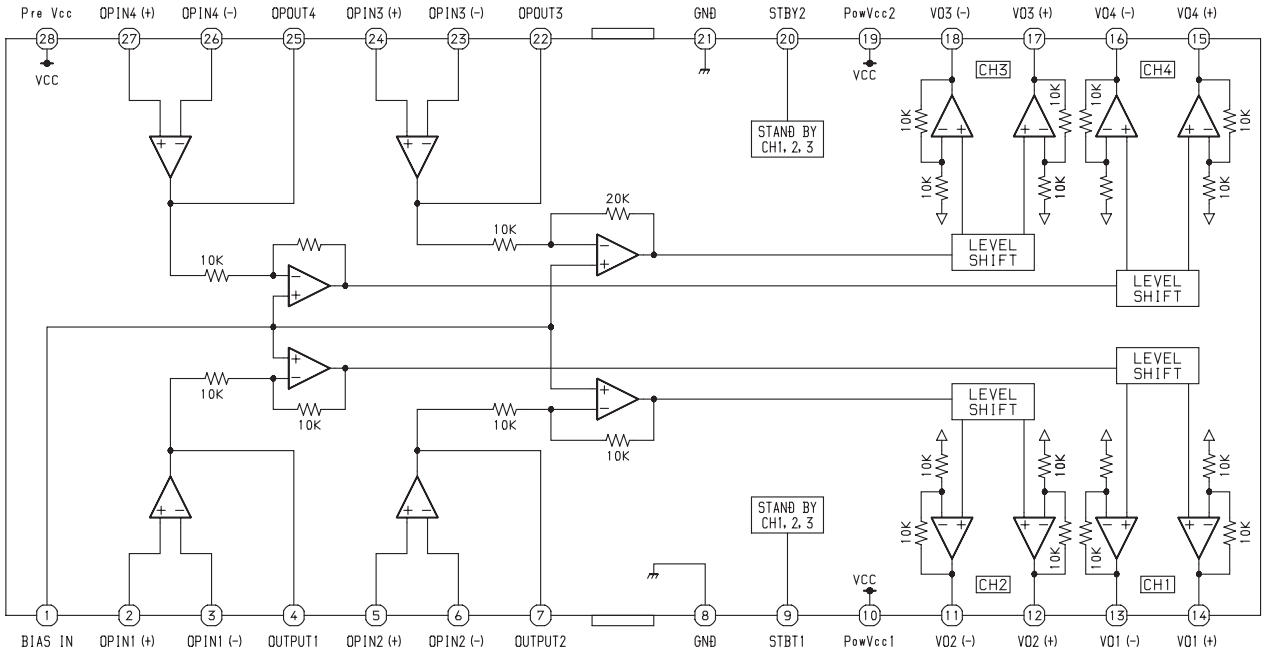
Pin No.	Pin Name	I/O	Description
78	P32	I	UP signal input from CN505 (SW509).
79	P33	I	JOG signal “JSW1” input CN505 (JS500).
80	P34	I	LEFT signal input from CN505 (SW509).

IC, XC9536-15VQ44C

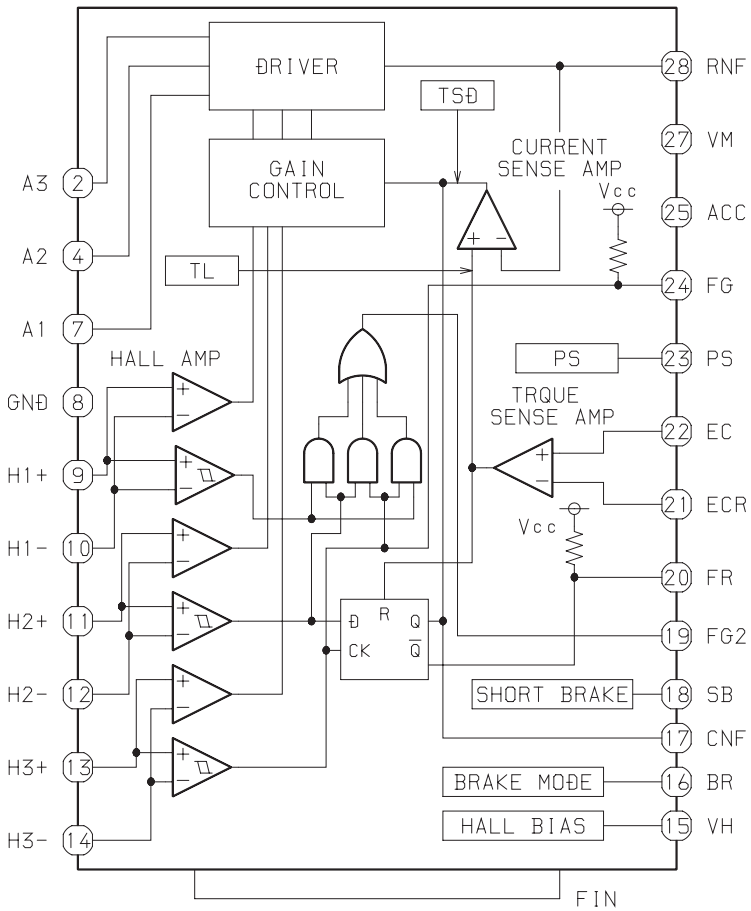
Pin No.	Pin Name	I/O	Description
1	SCART1	O	Wide disc playback high output (16:9 mode detect).
2	SCART2	O	DVD power on HIGH (HIGH signal output to SCART 8 pin, SCART enable).
3	TEST PIN	O	For software debugging.
4	GND	—	Ground.
5	PWR_CTL	O	Power control output to expander IC.
6	TEST PIN	O	For software debugging.
7	MPEG_CS	O	IC301 (MPEG IC, ZIBA-3) chip select.
8	DSP_CS	O	IC206 (DSP IC, GDC25D801) chip select.
9	TD1	I	JTAG program port for CPLD upgrade.
10	TMS	I	
11	TCK	I	
12	PP_CS	O	Software download adapter select.
13	CLOSE_SW	I	Tray limit SW input (LOW is input at tray close end position).
14	OPEN_SW	I	Tray limit SW input (LOW is input at tray open end position).
15	VCC	—	VCC.
16	SENSE	I	Interface signal for IC206 (DSP IC, GDC25D801).
17	GND	—	Ground.
18	ZISERR	I	EDC (Error detection & correction) signal input from IC206 (DSP IC, GDC25D801).
19	DAC_LO	O	Audio DAC latch strobe signal.
20	DINO_CS	O	Not used.
21	WR	I	IC108 (Main µ-COM, SH7034) bus write signal.
22	MICOM_WAIT	O	µ-COM WAIT signal.
23	MIC_ON	I	Karaoke MIC input.
24	TDO1	O	JTAG program port for CPLD Upgrade.
25	GND	—	Ground.
26	VCC	—	VCC.
27	RF_LAT	O	IC201 (RF IC, TA1254) serial interface latch signal.
28-30	A21-A19	I	IC108 (Main µ-COM, SH7034) address signal.
31	MPEG_WAIT	I	Wait signal from IC301. (MPEG IC, ZIBA-3)
32	LIMIT_SW	I	Sled limit switch input.
33	MICOM_RESET	I	µ-COM, expander reset signal input.
34	EXP_W2	O	IC103 (Expander, 74HC374) latch strobe.
35	VCC	—	VCC.
36	PWR_CTL	I	Power control input from IC500 (Front µ-COM).
37	MPEG_ERROR	O	EDC (Error detection & correction) signal output to IC301 (MPEG IC, ZIBA-3).
38	SENSE_MCOM	O	IC206 (DSP IC, GDC25D801) interface signal to IC108 (Main µ-COM, SH7034).
39-43	DO0-DO4	I/O	IC108 (Main µ-COM, SH7034) data bus.
44	IOCS1	I	IC101 (CPLD, XC9536) chip select from IC108 (Main µ-COM, SH7034).

IC BLOCK DIAGRAM

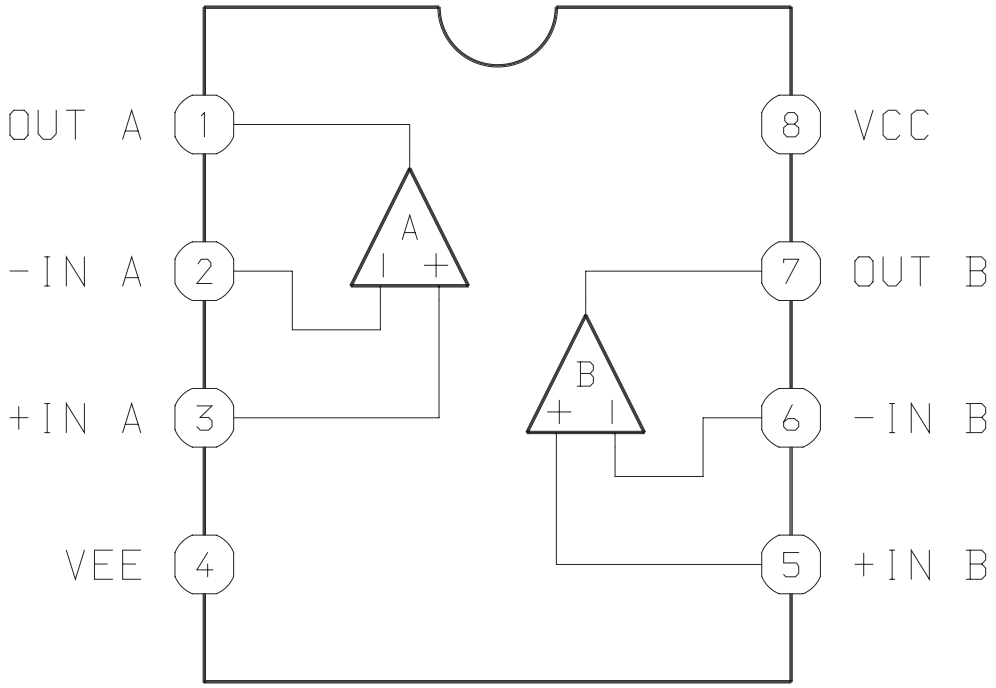
IC, BA5983FP



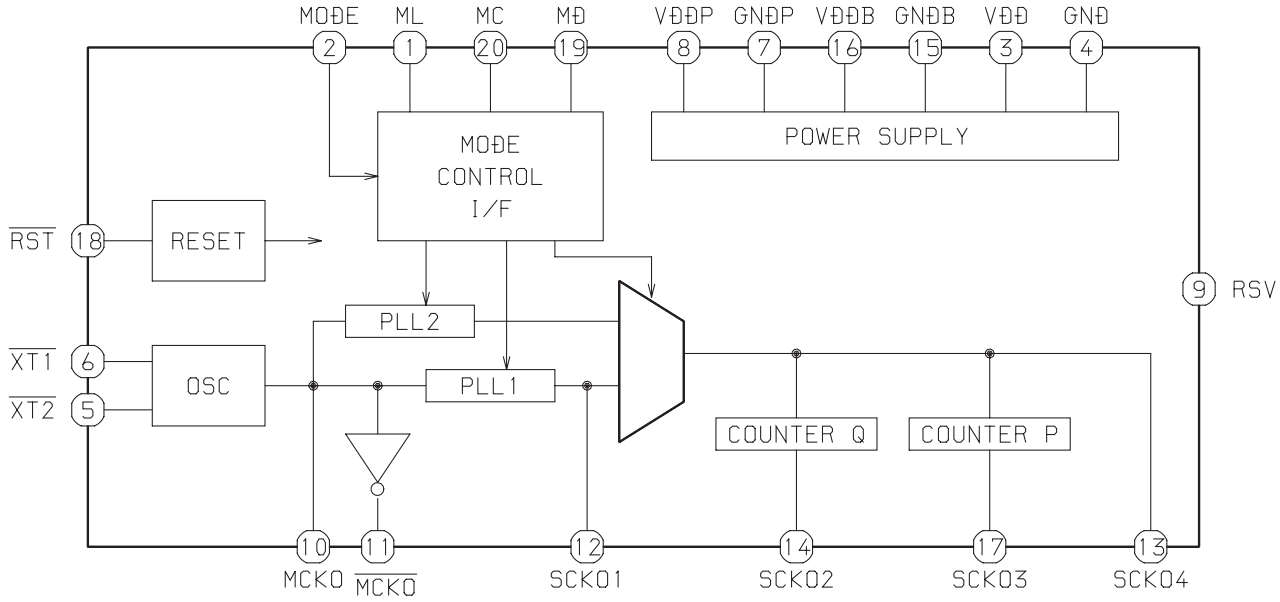
IC, BA6859AFP



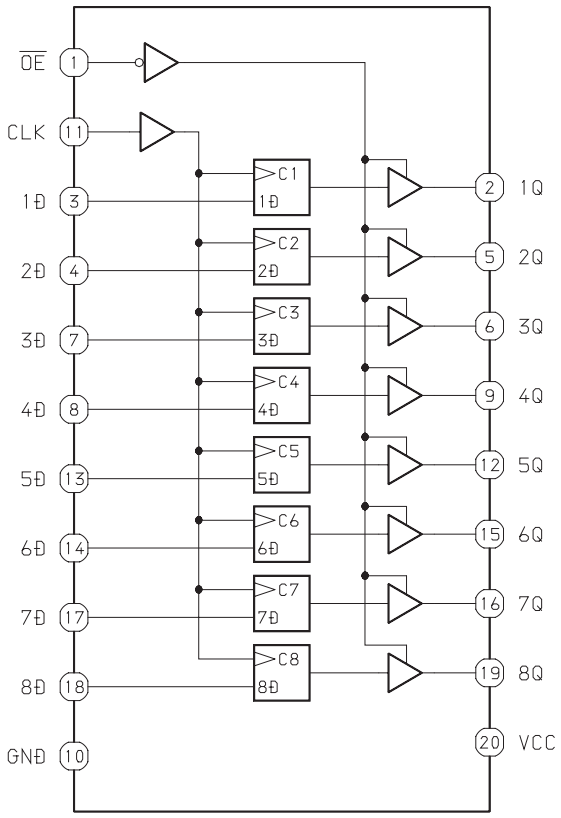
IC, KIA393F



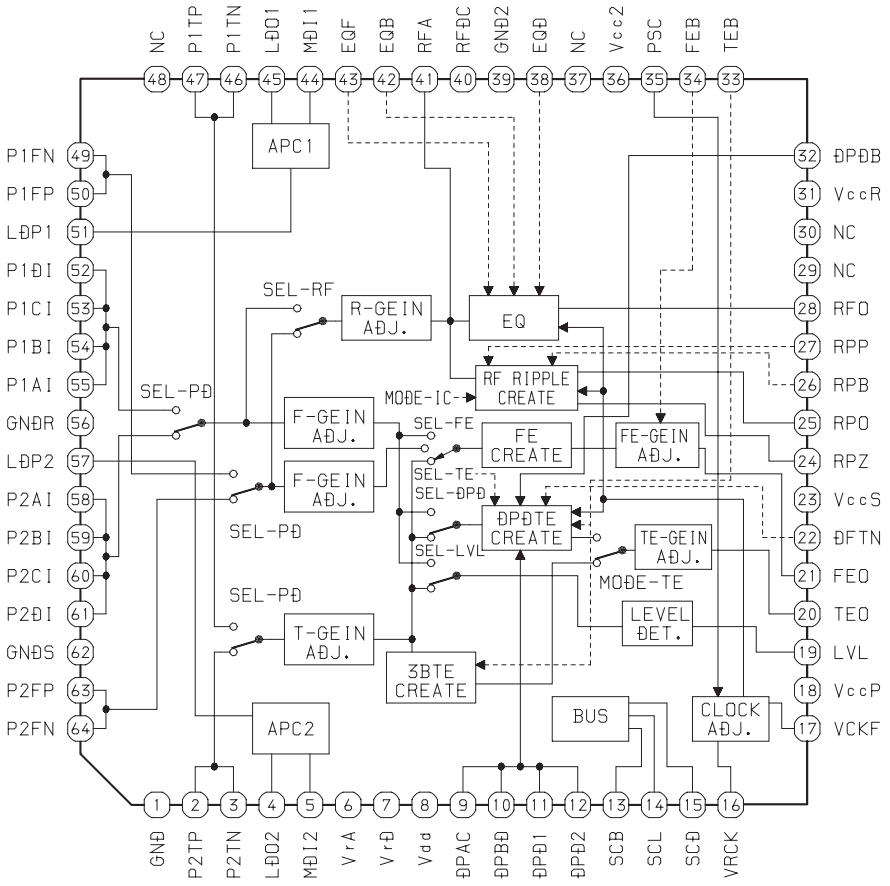
IC, PLL1700E



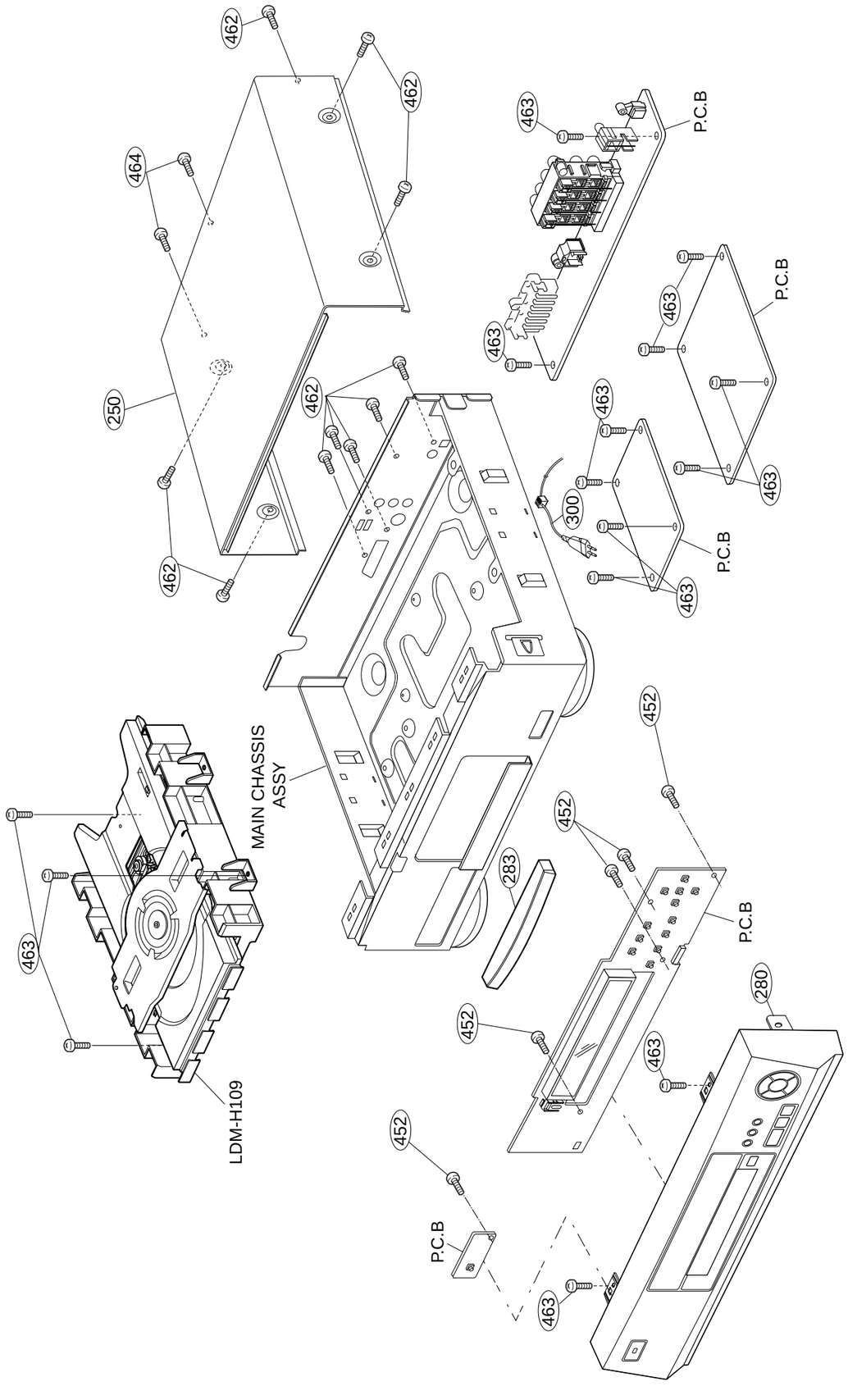
IC, SN74AHC374PWLE



IC, TA1254F



MECHANICAL EXPLODED VIEW 1/1



MECHANICAL PARTS LIST 1/1

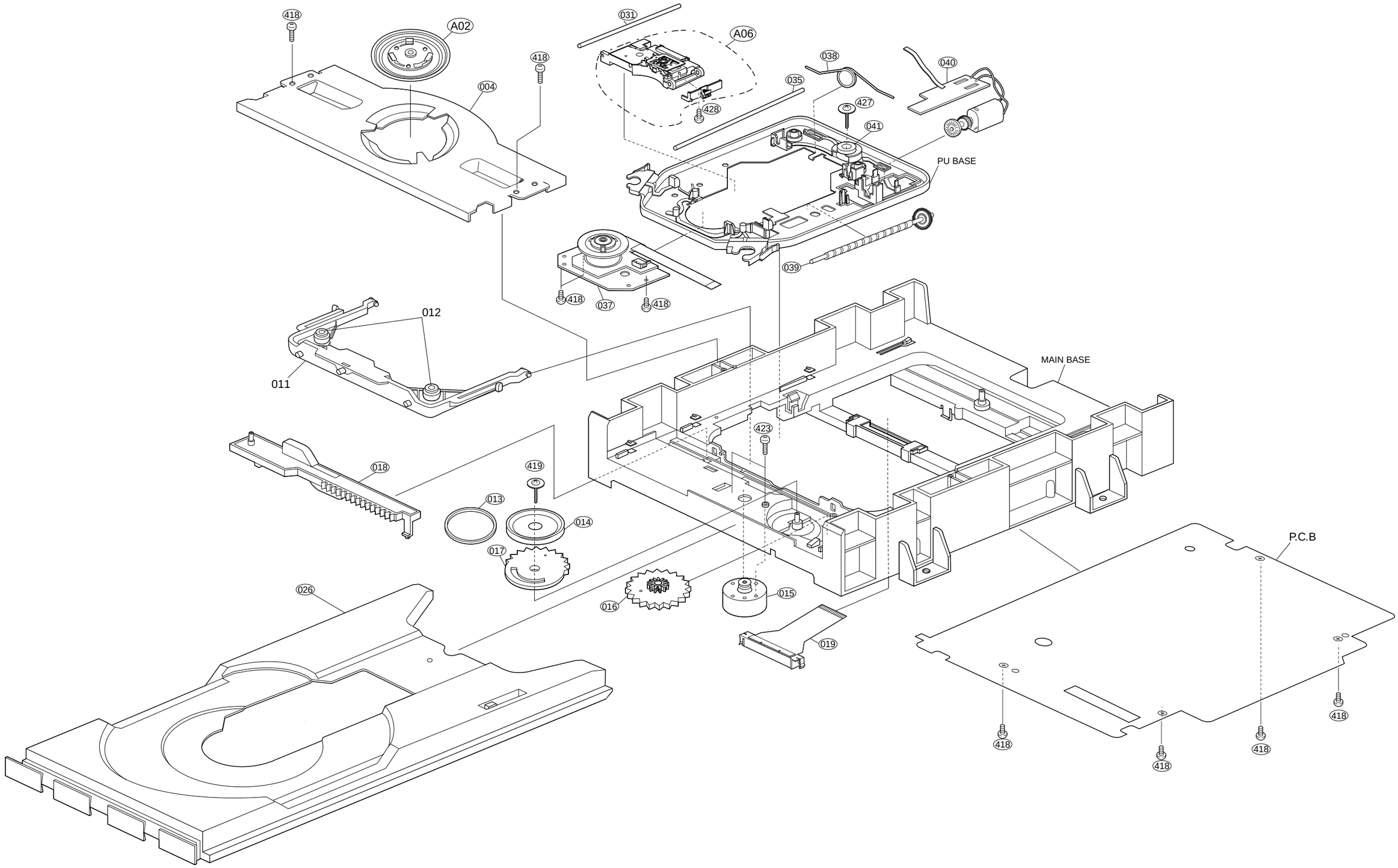
DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
250	S1-10R-014-3A0		CASE TOP
280	S7-21R-F12-5A0		PANEL ASSY FRONT[NO
283	S5-81R-000-7A0		TRAY DOOR ASSY
300	S4-10R-AHC-02B		NI NM CORE SP-2 1 POW<EZ>
452	S3-530-51A-000		SCREW,SPECIAL
462	S3-530-46K-000		SPECIAL SCREW 3-10 B.K
463	S3-530-51B-000		SPECIAL SCREW
464	S3-530-46N-000		SPECIAL SCREW 3-8 BK

COLOR NAME TABLE

Basic color symbol	Color	Basic color symbol	Color	Basic color symbol	Color
B	Black	C	Cream	D	Orange
G	Green	H	Gray	L	Blue
LT	Transparent Blue	N	Gold	P	Pink
R	Red	S	Silver	ST	Titan Silver
T	Brown	V	Violet	W	White
WT	Transparent White	Y	Yellow	YT	Transparent Yellow
LM	Metallic Blue	LL	Light Blue	GT	Transparent Green
LD	Dark Blue	DT	Transparent Orange		

MECHANISM EXPLODED VIEW 1/1



MECHANISM PARTS LIST 1/1

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
004	S8-10H-105-5A0		CLAMP,LDM-R608 BRACKET
011	S2-10H-101-1A0		FRAME UP/DOWN
012	S0-40H-103-9B0		RUBBER F(D2)
013	S4-00H-101-0A0		LOADING BELT
014	S4-70H-112-9A0		PULLEY GEAR
015	S6-81R-102-1A0		LOADING MOTOR ASSY
016	S4-70H-113-1A0		LOADING GEAR
017	S4-30H-000-4A0		LOADING CAM
018	S4-70H-113-0A0		EMERGENCY GEAR
019	S9-31H-000-3A0		HOLDER ASSY DECK ON
026	S3-90H-102-1A0		DISC TRAY
031	S3-70H-108-5B0		SHAFT PU SUB
035	S3-70H-108-5A0		SHAFT PU MAIN
037	S6-80H-B10-24B		MOTOR(MECH)
038	S9-70H-110-0A0		SPRING SKEW
039	S3-71H-100-9A0		LEAD SCREW SHAFT
040	S6-81H-102-0A0		PU FEED MOTOR ASSY
041	S0-40H-104-0B0		RUBBER R(D2)
428	SS-ZZH-101-6A0		SCREW,+2.0-3.5
A02	S8-61H-001-1A0		DISC CLAMP ASSY
A06	S4-05H-108-0B0		MECHANISM ASSY

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